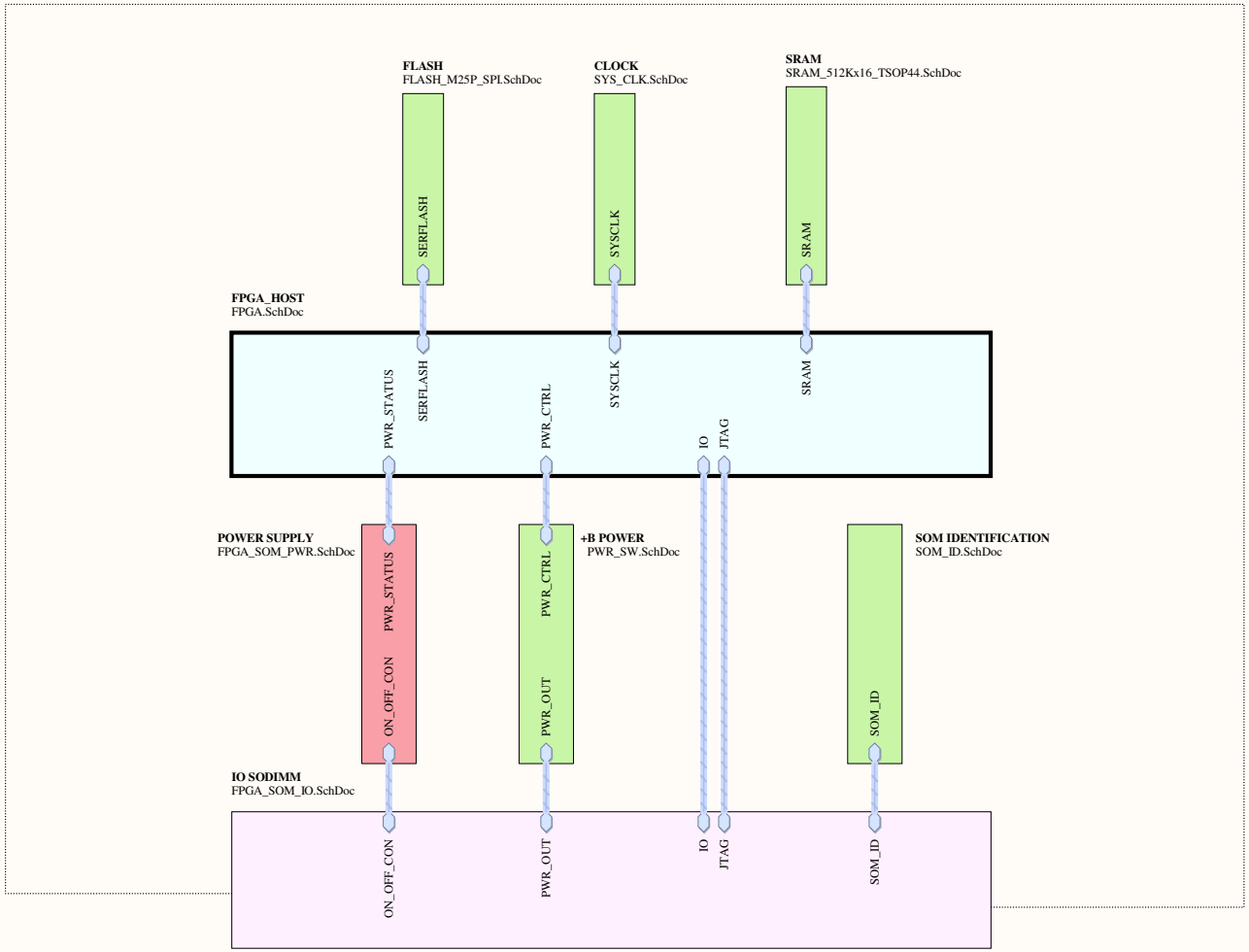
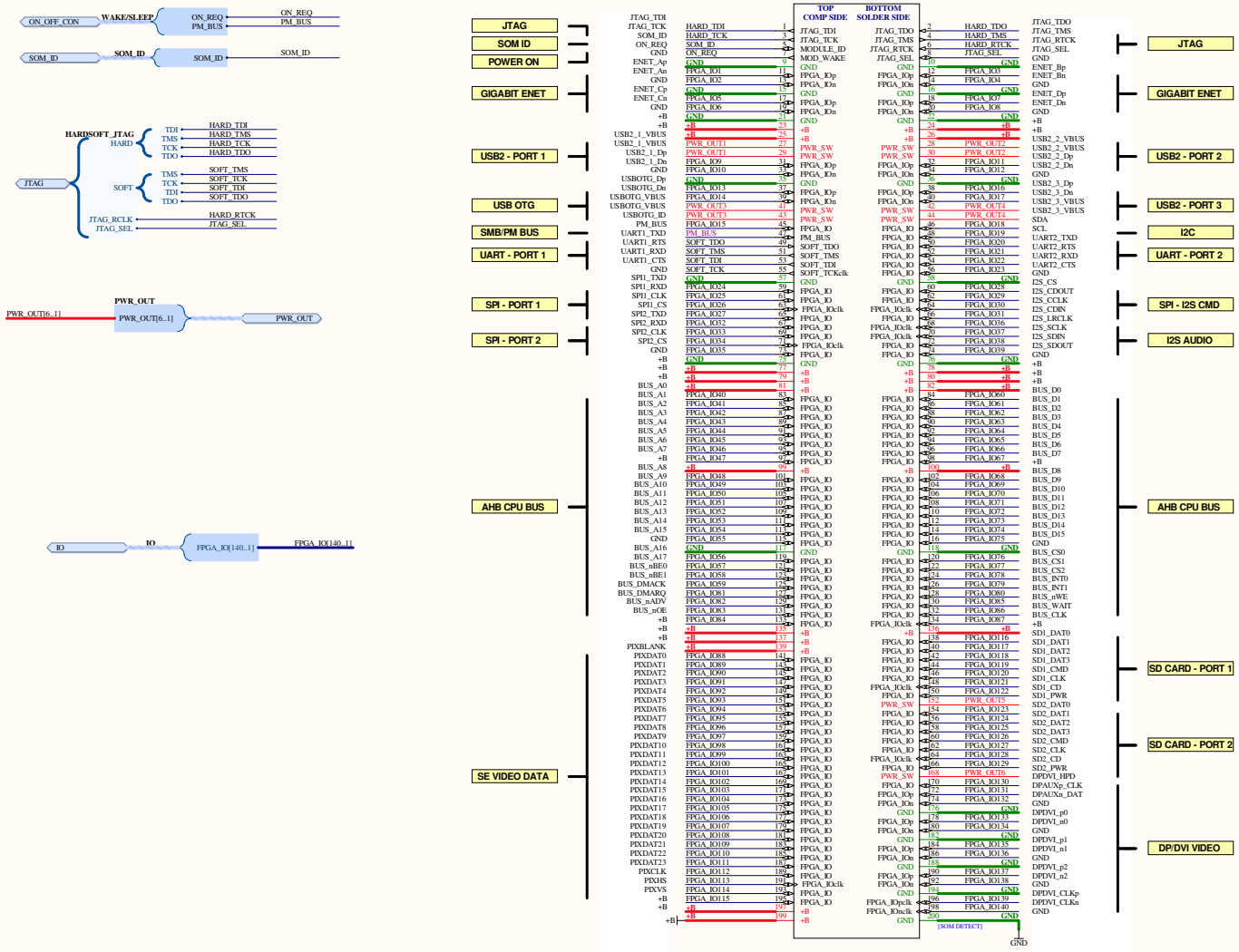


SODIMM

LOGO1

PCB1
SOM03 Blank PCB
Printed Circuit Board (Bare)

Title		
Size: A3	Number	Revision
Date: 23/09/2011	Sheet of	
File: C:\SRKH\SOM03 - XC3S1600E\SOM03_Hw.ddb	Drawn By:	



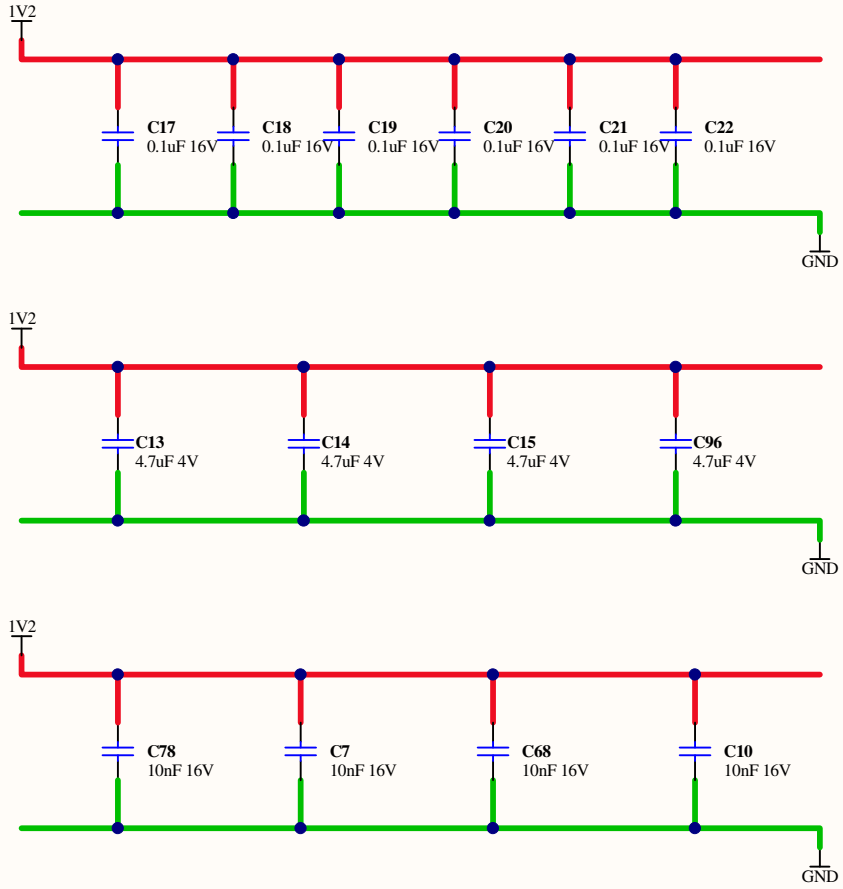
SOM PIN DESCRIPTIONS:

SERVICES:

- 18x 4.5V TO 5.5V POWER PINS (5.4AMPS)
- 140x SINGLE ENDED 3.3V IO
- 13x DIFFERENTIAL PAIRS
- 11x SINGLE ENDED GLOBAL CLOCKS
- 1x DIFFERENTIAL GLOBAL CLOCK
- 4x 5VDC 600mA POWER OUTPUTS (ie USB PORT POWER)
- 2x 3.3VDC 600mA POWER OUTPUTS (ie SDCARD POWER)
- PLUG PACK DETECT/MONITOR (PMBUS)
- SOM ID ROM (SOM ID)
- HARD JTAG WITH ADAPTIVE CLOCKING OPTION
- SOM JTAG CONTROLLER DETECT AND BUS REQUEST (JTAG SEL)

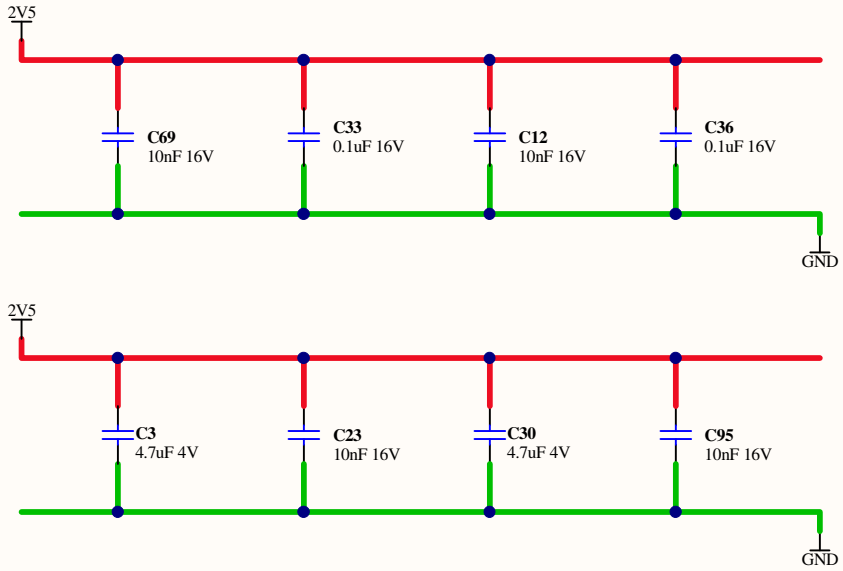
POWER HANDLING CAPACITY
MAX VOLTAGE PER PIN: 25V
MAX CURRENT PER PIN: 0.3A
NUMBER OF POWER PINS: GND x 19/+B x 18
MAX MODULE POWER: 27W (5V @ 5.4A)

Title		
Size: A2	Number	Revision
Date: 23/09/2011		Sheet of
File: C:\SRKH\..\FPGA_SOM_IO.SchDoc		Drawn By:



Sheet Title	*FPGA Bypass 2V5*		
Project Title	*SOM02*		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 3 of 13	
File: FPGA_Bypass_FPGA_1V2.SchDoc			

Altium Limited
3 Minna Close
Belrose
NSW 2085
Australia



Sheet Title	***FPGA Bypass 2V5***		
Project Title	***SOM02***		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 4 of 13	
File: FPGA_Bypass_FPGA_2V5.SchDoc			

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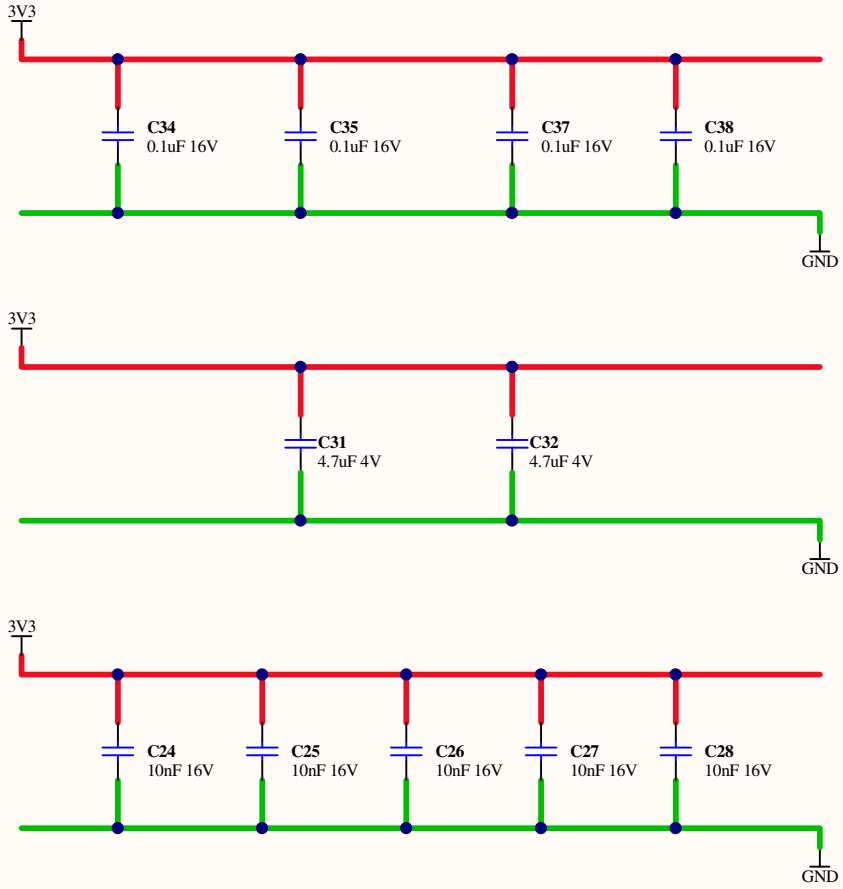
Belrose
NSW 2085
Australia



Sheet Title	***FPGA Bypass 2V5***		
Project Title	***SOM02***		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 5 of 13	
File: FPGA_Bypass_FPGA_3V3.SchDoc			

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Belrose
NSW 2085
Australia

Altium

SRAM - 64K/256K x 16

SRAM-256Kx16

SRAM

A[18..0] D[15..0] NCS NWE NOE NBHE NBLE

SRAM_A[18..0] SRAM_D[15..0] SRAM_NCS SRAM_NWE SRAM_NOE SRAM_NBHE SRAM_NBLE

IO — IO — FPGA_IO[140..1] — FPGA_IO[140..1]

SYSCLK — SYSCLK — 24MHZ

WAKE/SLEEP

PWR_STATUS — ON_REQ PM_BUS — ON_REQ PM_BUS

HARDSOFT_JTAG

JTAG — HARD: TDI TMS TCK TDO — HARD_TDI HARD_TMS HARD_TCK HARD_TDO

SOFT: TMS TCK TDI TDO — SOFT_TMS SOFT_TCK SOFT_TDI SOFT_TDO

JTAG_RCLK JTAG_SEL — HARD_RTCK JTAG_SEL

R2 5R6 1%

FPGA_NonIO — FPGA_NonIO.SchDoc

TDI TMS TCK TDO FBTCK

GCLK0
FPGA SYSTEM CLOCK IS ON GLOBAL CLOCK 0
24MHZ

1V2

FPGA_DECOUPLING_CAPS_1V2
FPGA_Bypass_FPGA_1V2.SchDoc

2V5

FPGA_DECOUPLING_CAPS_2V5
FPGA_Bypass_FPGA_2V5.SchDoc

3V3

FPGA_DECOUPLING_CAPS_3V3
FPGA_Bypass_FPGA_3V3.SchDoc

PWR_CTRL[6..1] — PWR_CTRL — PWR_CTRL[6..1] — PWR_CTRL

XILINX MULTIBOOT COMPATIBLE
GOLDEN

SERFLASH — SERFLASH — FLASH_CS_N DOUT DIN SCLK — FLASH_GOLD_CS_N FLASH_GOLD_DOUT FLASH_GOLD_DIN FLASH_GOLD_CLK

FPGA WILL ATTEMPT SPI BOOT THREE TIMES (UG332-P227)

NOTE:
INIT_B ASSERTS DURING CONFIG.
DOUT OSCILLATES DURING CONFIG.

U3A — XC3S1600E-4FGG400C — BANK 0

IO_L01P_0	C17	SRAM_D14
IO_L01N_0	D17	SRAM_D7
IO_L03P_0	A19	SRAM_D3
IO_L03N_0/VREF_0	A18	SRAM_D5
IO	E16	SRAM_NBLE
IO_L04P_0	A16	SRAM_D15
IO_L04N_0	A17	SRAM_D13
IO_L06P_0	B15	SRAM_D2
IO_L06N_0	A15	SRAM_NOE
IO	E14	JTAG_SEL
IO_L07P_0	D14	SRAM_D6
IO_L07N_0	C14	SRAM_D4
IO_L09P_0	A14	SRAM_D12
IO_L09N_0/VREF_0	A13	SRAM_A7
IO	E13	FPGA_IO15
IO_L10P_0	C13	SRAM_A6
IO_L10N_0	B13	SRAM_NWE
IO	E13	SRAM_A5
IO_L12P_0	D12	SOFT_TMS
IO_L12N_0	C12	SRAM_D11
IO	A12	SRAM_D10
IO_L13P_0	C12	FPGA_IO1
IO_L13N_0	B12	FPGA_IO2
IO_L15P_0/GCLK4	C11	FPGA_IO26
IO_L15N_0/GCLK5	D11	FPGA_IO28
IO/VREF_0	C11	SRAM_D9
IO_L16P_0/GCLK6	E11	FPGA_IO34
IO_L16N_0/GCLK7	E10	FPGA_IO37
IO_L18P_0/GCLK10	A9	FPGA_IO36
IO_L18N_0/GCLK11	C10	IONC30
IO	B9	FPGA_IO7
IO_L19P_0	B9	FPGA_IO8
IO_L19N_0	D9	FPGA_IO19
IO_L21P_0	B9	SRAM_A18
IO_L21N_0	A8	SRAM_A8
IO	B9	FPGA_IO5
IO_L22P_0	D8	FPGA_IO6
IO_L22N_0/VREF_0	D8	SRAM_A13
IO	A8	FPGA_IO3
IO_L24P_0	C7	FPGA_IO4
IO_L24N_0/VREF_0	C7	SRAM_A9
IO	A7	FPGA_IO11
IO_L25P_0	A6	FPGA_IO12
IO_L25N_0	B6	FPGA_IO16
IO_L27P_0	B5	FPGA_IO17
IO_L27N_0	C7	SRAM_A14
IO	C6	FPGA_IO9
IO_L28P_0	D6	FPGA_IO10
IO_L28N_0	C5	SOFT_TDO
IO_L30P_0	C5	SRAM_A11
IO_L30N_0/VREF_0	A3	FPGA_IO21
IO	B2	FPGA_IO13
IO_L31P_0	C5	SRAM_A12
IO_L31N_0	A2	FPGA_IO14
IO_L32P_0	C4	SOFT_TDI
IO_L32N_0/HSWAP	D4 (OUTPUT ONLY)	SRAM_A12

R21 1K 1%

GND

HSWAP (INT PULLED UP VIA FIXED RESISTOR)
HSWAP HIGH = INT PULLUPS OFF
HSWAP LOW= INT PULLUPS ON
(DS312-P72)

[HSWAP]
HSWAP = L
EXTERNAL PULL DOWN
TO ENABLE PULL UP RESISTORS
ON ALL IO

INTERNAL XC3SxxxE RESISTANCE VALUES
RPU - PULL UP RESISTOR (VCCO = 3V3) = 10K8 OHMS
RPD - PULL DOWN RESISTOR (VCCO = 3V3) = 54K5 OHMS

U3B — XC3S1600E-4FGG400C — BANK 1

IO_L01P_1/A16	U17	PWR_CTRL4
IO_L01N_1/A15	T17	FPGA_IO59
IO_L02P_1/A14	T17	IONC0
IO_L02N_1/A13	T18	FPGA_IO60
IO_L03P_1	T19	FPGA_IO62
IO_L03N_1/VREF_1	T19	FPGA_IO114
IO_L04P_1	V20	ON_REQ
IO_L04N_1	W20	FPGA_IO110
IO_L05P_1	R17	IONC2
IO_L05N_1	R18	FPGA_IO112
IO_L06P_1	U20	PM_BUS
IO_L06N_1	P20	IONC3
IO_L07P_1	P17	IONC4
IO_L07N_1	P18	PWR_CTRL5
IO_L08P_1	R20	FPGA_IO101
IO_L08N_1/VREF_1	P20	FPGA_IO117
IO_L09P_1	N16	FPGA_IO109
IO_L09N_1	P16	FPGA_IO107
IO_L10P_1	N18	IONC6
IO_L10N_1	N19	IONC7
IO_L11P_1	M15	FPGA_IO83
IO_L11N_1	M15	IONC5
IO_L12P_1/A12	M17	FPGA_IO108
IO_L12N_1/A11	M18	FPGA_IO111
IO_L13P_1	M19	IONC8
IO_L13N_1/VREF_1	L19	FPGA_IO67
IO_L14P_1/A10/RHCLK0	M16	FPGA_IO115
IO_L14N_1/A9/RHCLK1	N17	IONC9
IO_L15P_1/A8/RHCLK2	L17	IONC10
IO_L15N_1/A7/RHCLK3/TRDY1	L14	IONC11
IO_L16P_1/A6/RHCLK4/IRDY1	K13	IONC12
IO_L16N_1/A5/RHCLK5	K14	IONC13
IO_L17P_1/A4/RHCLK6	K20	FPGA_IO18
IO_L17N_1/A3/RHCLK7	J20	IONC15
IO_L18P_1/A2	J16	SRAM_A15
IO_L18N_1/A1	J16	FPGA_IO20
IO_L19P_1	J14	IONC17
IO_L19N_1/A0	L3	IONC18
IO_L20P_1	J18	SRAM_D8
IO_L20N_1	J19	IONC16
IO_L21P_1	J19	IONC20
IO_L21N_1	H16	IONC23
IO_L22P_1	H15	IONC14
IO_L22N_1	H17	IONC21
IO_L23P_1	H18	IONC22
IO_L23N_1	E20	SRAM_NBHE
IO_L24P_1	E20	SRAM_D1
IO_L24N_1/VREF_1	E16	FPGA_IO33
IO_L25P_1	E16	IONC24
IO_L25N_1	D20	SRAM_A0
IO_L26P_1	D19	SRAM_A16
IO_L26N_1	E17	IONC1
IO_L27P_1	E18	SRAM_NCS
IO_L27N_1	E20	SRAM_D0
IO_L28P_1	D20	SRAM_A1
IO_L28N_1	D18	SRAM_A2
IO_L29P_1/HDC	D18	SRAM_A17
IO_L29N_1/LDC0	C20	SRAM_A4
IO_L30P_1/LDC1	W2	SRAM_A3
IO_L30N_1/LDC2	T19	

R2 5R6 1%

U3C — XC3S1600E-4FGG400C — BANK 2

IO_L01P_2/CSO_B	U4	FLASH_GOLD_CS_N
IO_L01N_2/INIT_B	V4	FPGA_IO91
IO_L03P_2/DOUT/BUSY	U5 (OUTPUT ONLY)	IONC25
IO_L03N_2/MOSI/CSI_B	V5	FLASH_GOLD_DIN
IO/VREF_2	T3	FPGA_IO89
IO_L04P_2	W4	FPGA_IO120
IO_L04N_2	Y4	FPGA_IO93
IO_L06P_2	V5	FPGA_IO122
IO_L06N_2	U6	PWR_CTRL6
IO	Y5	FPGA_IO123
IO_L07P_2	V7	FPGA_IO124
IO_L07N_2	U7	FPGA_IO126
IO_L09P_2	R7	FPGA_IO96
IO_L09N_2/VREF_2	R7	FPGA_IO92
IO	Y7	FPGA_IO99
IO_L10P_2	W8	FPGA_IO95
IO_L10N_2	V8	FPGA_IO125
IO	R8	FPGA_IO97
IO_L12P_2	V9	FPGA_IO79
IO_L12N_2	R9	FPGA_IO129
IO	R9	FPGA_IO127
IO_L13P_2	Y9	FPGA_IO98
IO_L13N_2	R8	IONC26
IO_L15P_2/D7/GCLK12	W9	FPGA_IO139
IO_L15N_2/D6/GCLK13	W10	FPGA_IO140
IO/D5	N11	FPGA_IO100
IO_L16P_2/D4/GCLK14	R10	FPGA_IO121
IO_L16N_2/D3/GCLK15	P10	FPGA_IO113
IO_L18P_2/D2/GCLK2	T10	FPGA_IO87
IO_L18N_2/D1/GCLK3	V11	FPGA_IO103
IO/M1	F11	HOST_M1
IO_L19P_2/M0	F11	HOST_M0
IO_L19N_2/DIN/D0	T12	FLASH_GOLD_DOUT
IO_L21P_2	V12	FPGA_IO137
IO_L21N_2	U12	FPGA_IO138
IO	W13	IONC27
IO_L22P_2	W12	PWR_CTRL6
IO_L22N_2/VREF_2	W12	PWR_CTRL2
IO	R13	FPGA_IO104
IO_L24P_2	V13	FPGA_IO131
IO_L24N_2	U13	FPGA_IO132
IO	T13	FPGA_IO105
IO_L25P_2	R14	FPGA_IO106
IO_L25N_2	U14	IONC28
IO_L27P_2/A23	V15	FPGA_IO135
IO_L27N_2/A22	T14	FPGA_IO136
IO	W15	PWR_CTRL3
IO_L28P_2	U15	FPGA_IO133
IO_L28N_2	T15	FPGA_IO134
IO_L30P_2/A21	U16	FPGA_IO130
IO_L30N_2/A20	V16	FPGA_IO103
IO/VREF_2	Y17	IONC19
IO_L31P_2/VS2/A19	W18	HOST_VS0
IO_L31N_2/VS1/A18	R18	HOST_VS1
IO_L32P_2/VS0/A17	Y19	HOST_VS2
IO_L32N_2/CCLK	W19	FLASH_GOLD_CLK

U3D — XC3S1600E-4FGG400C — BANK 3

IO_L01P_3	D3	FPGA_IO24
IO_L01N_3	E2	FPGA_IO29
IO_L02P_3	E3	SRAM_A10
IO_L02N_3/VREF_3	E1	FPGA_IO25
IO_L03P_3	D1	FPGA_IO23
IO_L03N_3	D1	FPGA_IO27
IO_L04P_3	E1	FPGA_IO31
IO_L04N_3	F4	FPGA_IO38
IO_L05P_3	F3	FPGA_IO32
IO_L05N_3	F2	FPGA_IO35
IO_L06P_3	F1	FPGA_IO39
IO_L06N_3	G3	FPGA_IO60
IO_L07P_3	G4	FPGA_IO40
IO_L07N_3	F5	FPGA_IO63
IO_L08P_3	G5	FPGA_IO41
IO_L08N_3	E5	FPGA_IO61
IO_L09P_3	H3	FPGA_IO42
IO_L09N_3/VREF_3	H5	FPGA_IO62
IO_L10P_3	H7	IONC29
IO_L10N_3	F1	FPGA_IO45
IO_L11P_3	H4	FPGA_IO43
IO_L11N_3	H2	FPGA_IO47
IO_L12P_3	J1	FPGA_IO66
IO_L12N_3	G6	FPGA_IO65
IO_L13P_3	J5	FPGA_IO44
IO_L13N_3	K3	FPGA_IO49
IO_L14P_3/LHCLK0	K2	FPGA_IO68
IO_L14N_3/LHCLK1	K1	FPGA_IO64
IO_L15P_3/LHCLK2	K7	FPGA_IO67
IO_L15N_3/LHCLK3/IRDY2	M1	FPGA_IO69
IO_L16P_3/LHCLK4/TRDY2	L4	FPGA_IO48
IO_L16N_3/LHCLK5	M3	FPGA_IO52
IO_L17P_3/LHCLK6	L3	FPGA_IO70
IO_L17N_3/LHCLK7	M8	FPGA_IO76
IO_L18P_3	M6	FPGA_IO51
IO_L18N_3	M5	FPGA_IO71
IO_L19P_3	M4	FPGA_IO50
IO_L19N_3	M6	FPGA_IO73
IO_L20P_3	N6	FPGA_IO57
IO_L20N_3/VREF_3	N1	FPGA_IO72
IO_L21P_3	N2	FPGA_IO54
IO_L21N_3	N7	FPGA_IO119
IO_L22P_3	P7	FPGA_IO84
IO_L22N_3/VREF_3	N3	FPGA_IO74
IO_L23P_3	P3	FPGA_IO55
IO_L23N_3	P1	FPGA_IO53
IO_L24P_3	R1	FPGA_IO75
IO_L24N_3	P5	FPGA_IO94
IO_L25P_3	R5	FPGA_IO81
IO_L25N_3	R2	FPGA_IO78
IO_L26P_3	T2	FPGA_IO118
IO_L26N_3	R3	FPGA_IO58
IO_L27P_3	R4	FPGA_IO56
IO_L27N_3	U1	FPGA_IO85
IO_L28P_3	T1	FPGA_IO77
IO_L28N_3/VREF_3	T3	FPGA_IO86
IO_L29P_3	T3	FPGA_IO116
IO_L29N_3	T2	FPGA_IO88
IO_L30P_3	V1	FPGA_IO90
IO_L30N_3	T4	

U3E — XC3S1600E-4FGG400C

IP_L29N_0	A4	INC0
IP_L29P_0	A5	INC1
IP_L26N_0	B6	INC2
IP_L26P_0	E7	INC3
IP_L23N_0	F8	INC4
IP_L23P_0	D8	INC5
IP_L20N_0	G9	INC6
IP_L20P_0	G8	INC7
IP_L17N_0/GCLK9	G10	INC8
IP_L17P_0/GCLK8	H10	24MHZ
IP_L14N_0	B11	INC10
IP_L14P_0	B12	INC11
IP_L11N_0	G14	INC12
IP_L11P_0	G13	INC13
IP_L08N_0	E14	INC14
IP_L08P_0	E15	INC15
IP_L05N_0	D15	INC16
IP_L05P_0	C15	INC17
IP_L02N_0	E16	INC18
IP_L02P_0	D16	INC19
IP	B18	INC20
IP	E5	INC21
IP	G18	INC22
IP	B20	INC23
IP	E19	INC24
IP/VREF_1	G15	INC25
IP	H14	INC26
IP	H15	INC27
IP	K18	INC28
IP/VREF_1	L18	INC29
IP	K19	INC30
IP	K20	INC31
IP	N14	INC32
IP	P15	INC33
IP	R19	INC34
IP	R16	INC35
IP	T16	INC36
IP_L29N_2	W16	INC37
IP_L29P_2	V16	INC38
IP_L26N_2	V14	INC39
IP_L26P_2	U15	INC40
IP_L23N_2/VREF_2	T13	INC41
IP_L23P_2	T14	INC42
IP_L20N_2	U12	INC43
IP_L20P_2	R12	INC44
IP_L17N_2/M2/GCLK1	P12	HOST_M2
IP_L17P_2/RDWR_B/GCLK0	P11	SOFT_TCK
IP_L14N_2/VREF_2	T10	INC45
IP_L14P_2	T9	INC46
IP_L11N_2	R8	INC47
IP_L11P_2	T8	INC48
IP_L08N_2	V6	INC49
IP_L08P_2	W6	INC50
IP_L05N_2	V6	INC51
IP_L05P_2	U6	INC52
IP_L02N_2	V2	INC53
IP_L02P_2	W2	INC54
IP	V3	INC55
IP	T4	INC56
IP	W1	INC57
IP/VREF_3	P6	INC58
IP	N5	INC59
IP	P3	INC60
IP	M2	INC61
IP	L5	INC62
IP	L8	INC63
IP/VREF_3	L6	INC64
IP	J5	INC65
IP	H1	INC66
IP	G1	INC67
IP	G6	INC68
IP	F5	INC69

M0, M1, M2
SET EXTERNAL SPI MASTER
BOOT FROM EXTERNAL SPI FLASH

M0 = H
EXTERNAL PULL UP
M1 = L
EXTERNAL PULL DOWN
M2 = L
EXTERNAL PULL DOWN
(UG332-P34)

XC3S1600E MODE PIN CONFIGURATIONS

M2_M1_M0	FUNCTION:
0 0 0	PLATFORM FLASH MODE
0 0 1	SPI MODE (MASTER)
0 1 0	BYTE PARALLEL INTERFACE
0 1 1	INTERNAL MASTER SPI FLASH
1 0 0	<RESERVED>
1 0 1	JTAG MODE
1 1 0	SLAVE PARALLEL
1 1 1	SLAVE SERIAL

XC3S1600E SPI MODE CONFIGURATIONS

VS2_VS1_VS0	FUNCTION:
0 0 0	<RESERVED>
0 0 1	<RESERVED>
0 1 0	<RESERVED>
0 1 1	<RESERVED>
1 0 0	<RESERVED>
1 0 1	(0x03) STANDARD READ
1 1 0	(0xE8) READ ARRAY
1 1 1	(0xBB) SPI FAST READ

M0 (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
EXT SPI BOOT MODE (MASTER)

M1 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
EXT SPI BOOT MODE (MASTER)

M2 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
EXT SPI BOOT MODE (MASTER)

VS0 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO_2

VS1 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO_2

VS2 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO_2

[M0]
M0 = H
INTERNAL PULL UP
BY HSWAP PRIOR TO
CONFIGURATION
(UG332-P47)
(UG332-P98)

SPI MODE (MASTER)
HOST_M0 — [M0] — R10 2K2 1% — 3V3

HOST_M1 — [M1] — R9 100R 1% — GND

HOST_M2 — [M2] — R8 100R 1% — GND

(0x0B) SPI FAST READ
HOST_VS0 — R7 2K2 1% — 3V3

HOST_VS1 — R6 2K2 1% — 3V3

HOST_VS2 — R5 2K2 1% — 3V3

[VS0, VS1, VS2]
VSx = H
INTERNAL PULL UP BY
HSWAP PRIOR TO CONFIG
VS = FAST READ (0x0B)
(UG332-P100)
(DS312-P79)
(UG332-P98)

Sheet Title	Host Controller - Spartan3AN-400		
Project Title	SOM02		
Size: A2	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 6 of 13	
File: FPGA.SchDoc			

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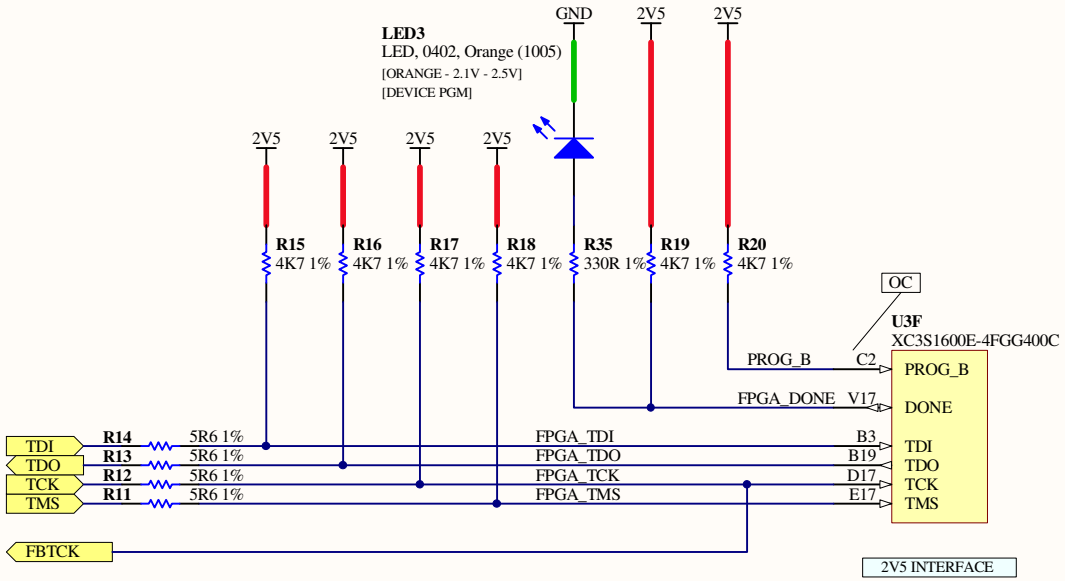
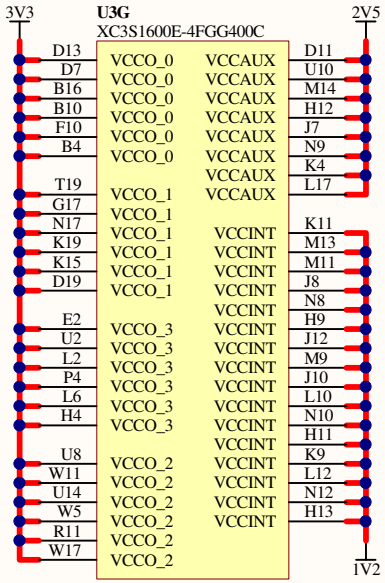


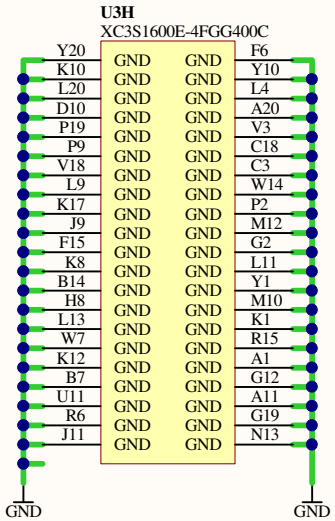
TDI, TDO, TCK AND TMS ALL REQUIRE SERIES RESISTOR FOR 3.3V OPERATION
(XAPP453-P13)

PROG_B (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
TO ALLOW CONFIGURATION TO START

DONE (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
HIGH = PROGRAM SUCCESSFUL

FPGA_DONE PIN
H = PROGRAMMED (LOADED)
INTERNAL PULL UP
LOW BY DEFAULT





Sheet Title	*HOST FPGA Pwr and Programming*		
Project Title	*SOM02*		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 7 of 13	
File: FPGA_NonIO.SchDoc			

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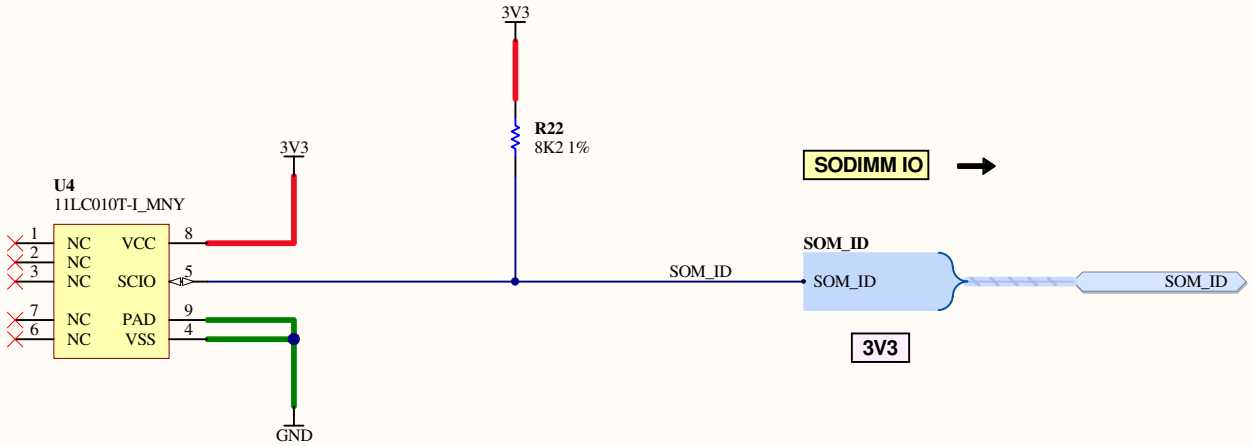
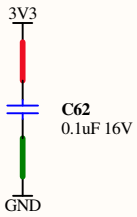
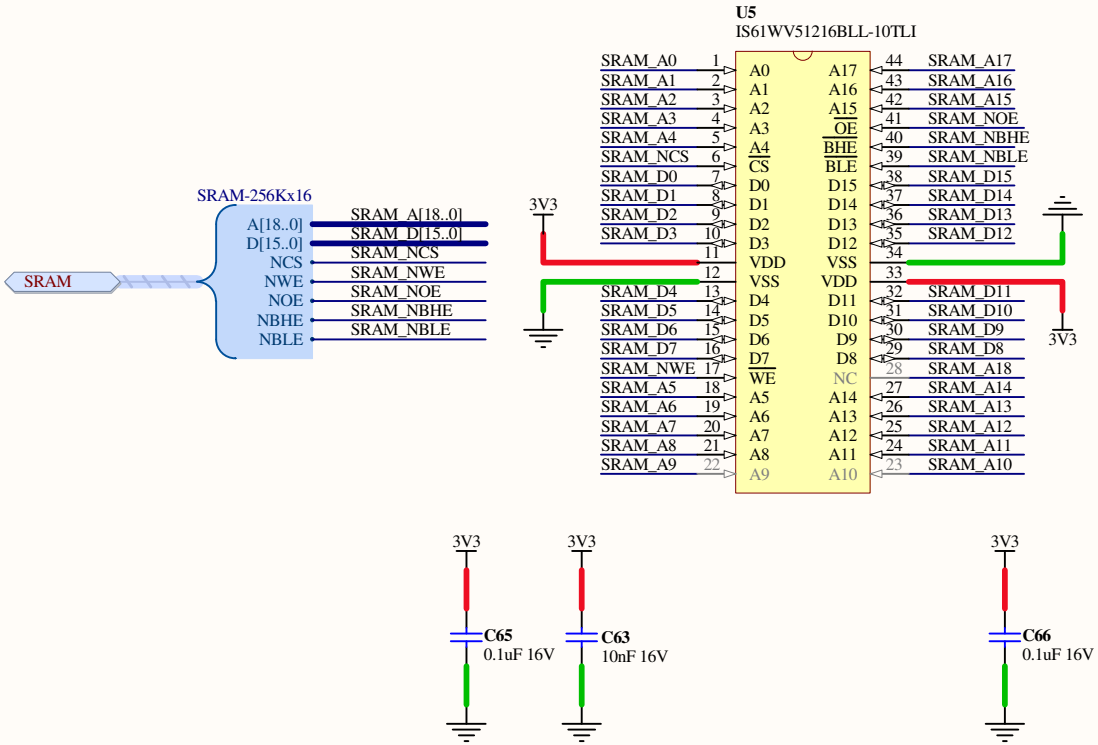




11LC010T-I_MNY POWER CONSUMPTION

STANDBY:	3V3	1uA
ACTIVE:	3V3	1mA

Title		
Size: A4	Number	Revision
Date: 23/09/2011	Sheet of	
File: C:\SRKH\SOM03 - XC3S1600E\SOM_ID.SchDoc	Drawn By:	



DEFAULT

IS61WV25616BLS FAST SRAM *(10nS)*
256K x16 BITS **512K bytes**

IS61WV51216BLL-10TLI FAST SRAM *(10nS)*
512K x16 BITS **1M bytes**

IS61WV20488BLL-10TLI FAST SRAM *(10nS)*
2048K x8 BITS **2M bytes**

Sheet Title	***256K x 16-Bit SRAM***		
Project Title	***SOM02***		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 9 of 0	
File: SRAM_512Kx16_TSOP44.SchDoc			

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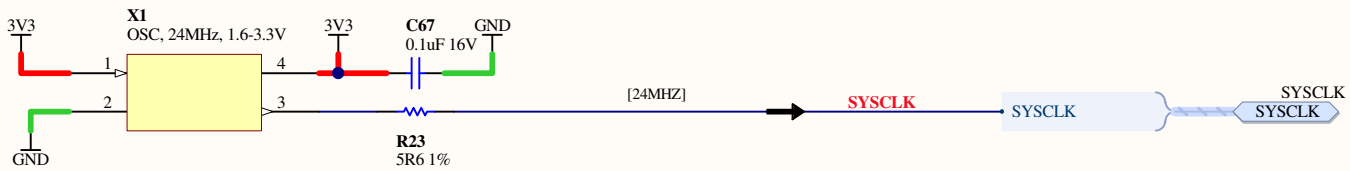

Sheet Title	*16M x 32 SDRAM TSOP54 x 2*		
Project Title	*SOM02*		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011 Time: 1:27:40 PM		Sheet 10 of 13	
File: SYS_CLK.SchDoc			

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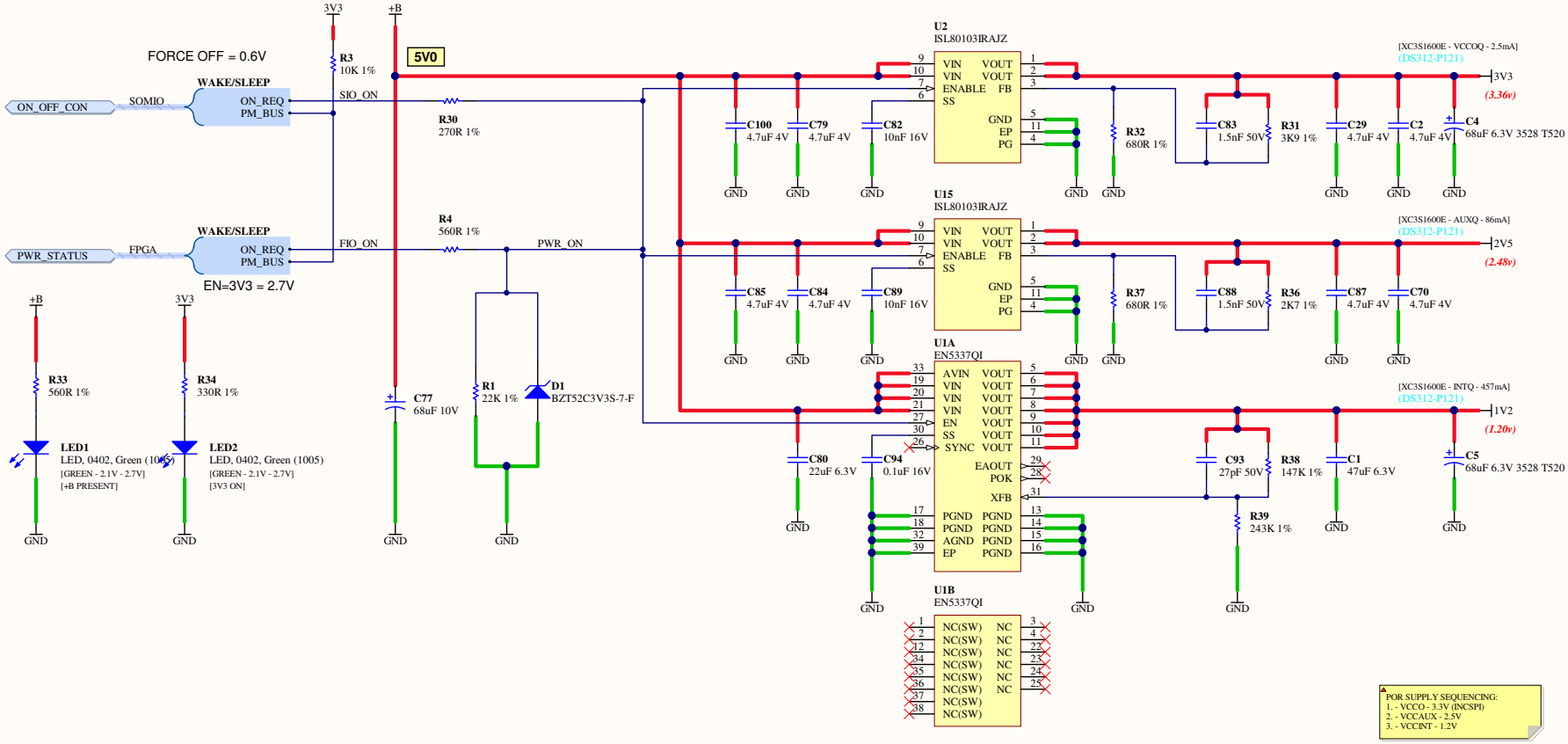
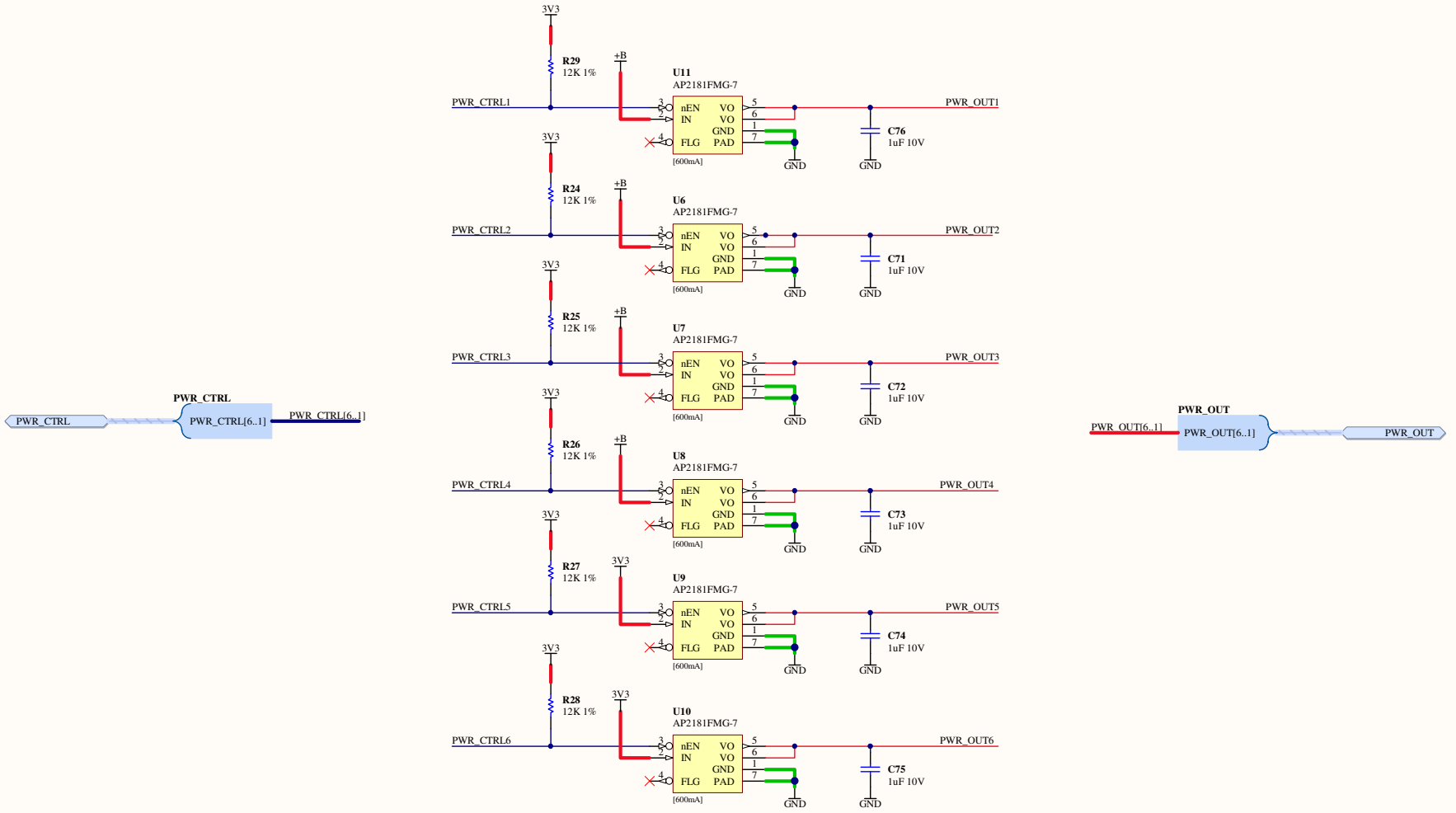
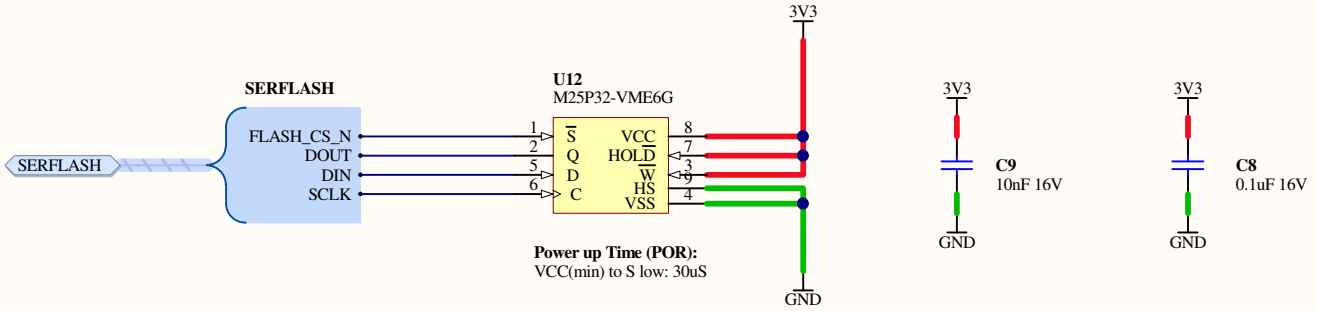

FORCE OFF = 0.6V
WAKE/SLEEP
ON_OFF_CON
SOMIO
ON_REQ
PM_BUS
SIO_ON
R3
10K 1%
3V3
+B
5V0
R30
270R 1%
WAKE/SLEEP
PWR_STATUS
FPGA
ON_REQ
PM_BUS
FIO_ON
R4
560R 1%
PWR_ON
EN=3V3 = 2.7V
R33
560R 1%
LED1
LED, 0402, Green (1005)
[GREEN - 2.1V - 2.7V]
[+B PRESENT]
R34
330R 1%
LED2
LED, 0402, Green (1005)
[GREEN - 2.1V - 2.7V]
[3V3 ON]
C77
68uF 10V
R1
22K 1%
D1
BZT52C3V3S-7-F
GND
U2
ISL80103IRAJZ
VIN
VOUT
ENABLE
FB
SS
GND
EP
PG
C100
4.7uF 4V
C79
4.7uF 4V
C82
10nF 16V
R32
680R 1%
C83
1.5nF 50V
R31
3K9 1%
C29
4.7uF 4V
C2
4.7uF 4V
C4
68uF 6.3V 3528 T520
[XC3S1600E - VCCOQ - 2.5mA]
(DS312-P121)
3V3
(3.36v)
U15
ISL80103IRAJZ
C85
4.7uF 4V
C84
4.7uF 4V
C89
10nF 16V
R37
680R 1%
C88
1.5nF 50V
R36
2K7 1%
C87
4.7uF 4V
C70
4.7uF 4V
[XC3S1600E - AUXQ - 86mA]
(DS312-P121)
2V5
(2.48v)
U1A
EN5337QI
AVIN
VOUT
VIN
EN
SS
SYNC
EAOUT
POK
XFB
PGND
AGND
EP
C80
22uF 6.3V
C94
0.1uF 16V
C93
27pF 50V
R38
147K 1%
C1
47uF 6.3V
C5
68uF 6.3V 3528 T520
[XC3S1600E - INTQ - 457mA]
(DS312-P121)
1V2
(1.20v)
R39
243K 1%
U1B
EN5337QI
NC(SW)
NC
POR SUPPLY SEQUENCING:
1. - VCCO - 3.3V (INCSPI)
2. - VCCAUX - 2.5V
3. - VCCINT - 1.2V


PWR_CTRL
PWR_CTRL
PWR_CTRL[6..1]
PWR_CTRL[6..1]
3V3
+B
R29
12K 1%
U11
AP2181FMG-7
PWR_CTRL1
nEN
IN
FLG
VO
VO
GND
PAD
[600mA]
PWR_OUT1
C76
1uF 10V
GND
R24
12K 1%
U6
AP2181FMG-7
PWR_CTRL2
PWR_OUT2
C71
1uF 10V
R25
12K 1%
U7
AP2181FMG-7
PWR_CTRL3
PWR_OUT3
C72
1uF 10V
R26
12K 1%
U8
AP2181FMG-7
PWR_CTRL4
PWR_OUT4
C73
1uF 10V
R27
12K 1%
U9
AP2181FMG-7
PWR_CTRL5
PWR_OUT5
C74
1uF 10V
R28
12K 1%
U10
AP2181FMG-7
PWR_CTRL6
PWR_OUT6
C75
1uF 10V
PWR_OUT
PWR_OUT[6..1]
PWR_OUT[6..1]
PWR_OUT



DEFAULT

M25P32-VME6G 32Mbit Serial PROM *(75MHz)*
33,554,432 BITS **4M bytes**
(ID=0x2016)

M25P64-VME6G 64Mbit Serial PROM *(75MHz)*
67,108,864 BITS **8M bytes**
(ID=0x2017)

M25P128-VME6G 128Mbit Serial PROM *(54MHz)*
134,217,728 BITS **16M bytes**
(ID=0x2018)

W25Q256FV 256Mbit Serial PROM *(80MHz)*
268,435,456 BITS **32M bytes**
(ID=0x4019)

Sheet Title: ***Host - Dual Serial Flash Memory***		
Project Title: ***SOM02***		
Size: A4	Assy: TBA	Revision: 04
Date: 23/09/2011 Time: 1:27:40 PM		Sheet 13 of 13
File: FLASH_M25P_SPI.SchDoc		

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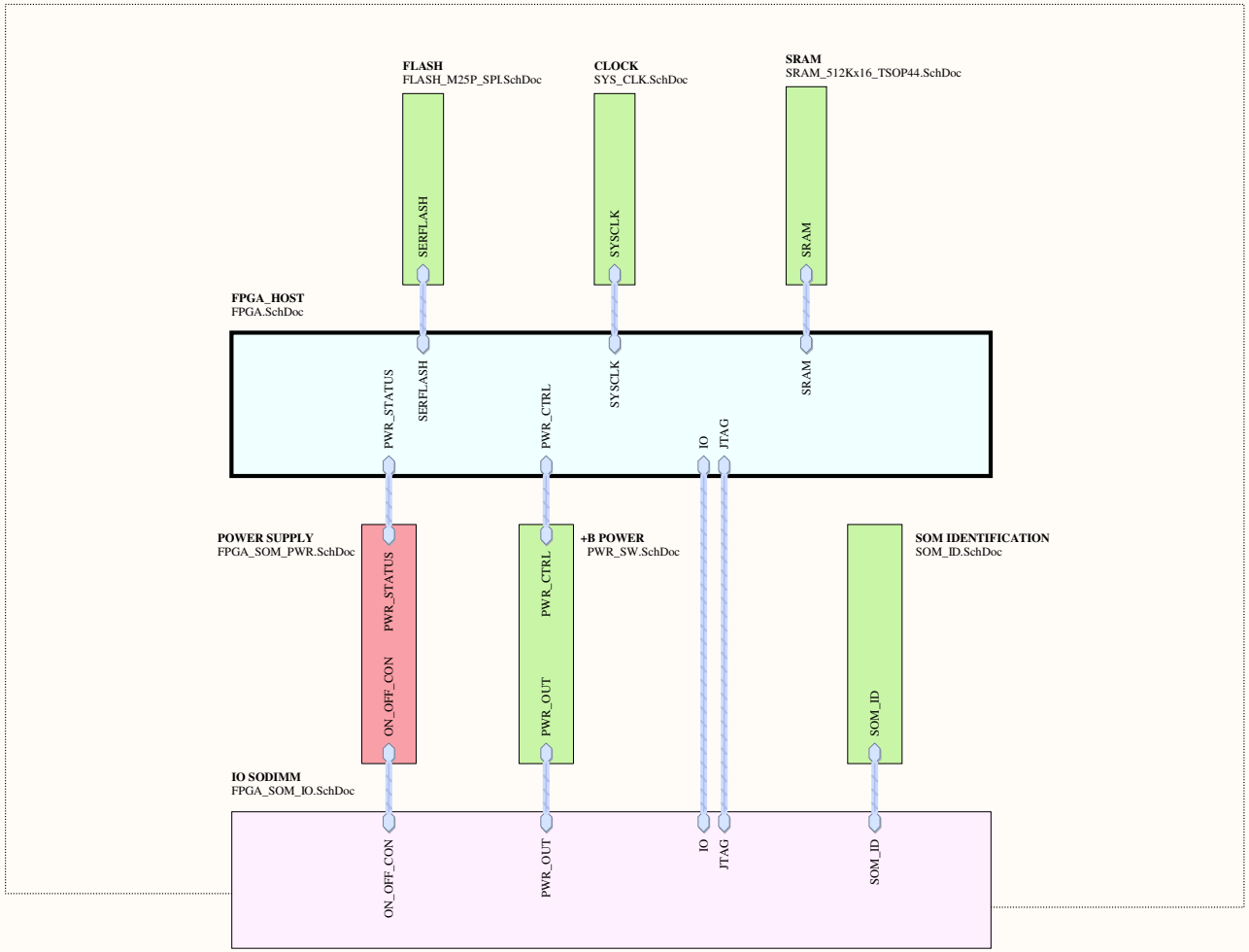
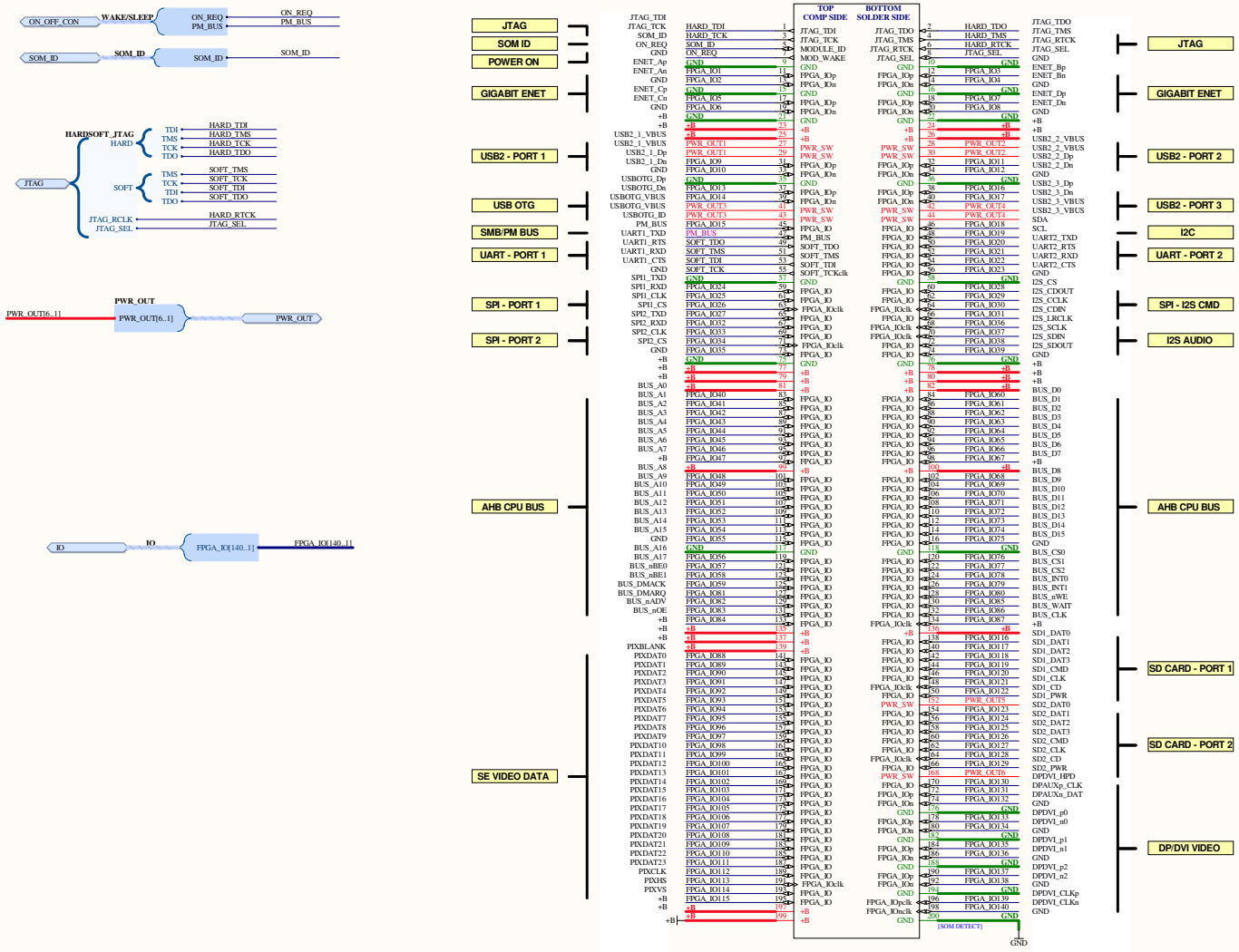


SODIMM

LOGO1

PCB1
SOM03 Blank PCB
Printed Circuit Board (Bare)

Title		
Size: A3	Number	Revision
Date: 23/09/2011	Sheet of	
File: C:\SRKH\SOM03 - XC3S1600E\SOM03_SODIMM.SchDoc	Drawn By:	



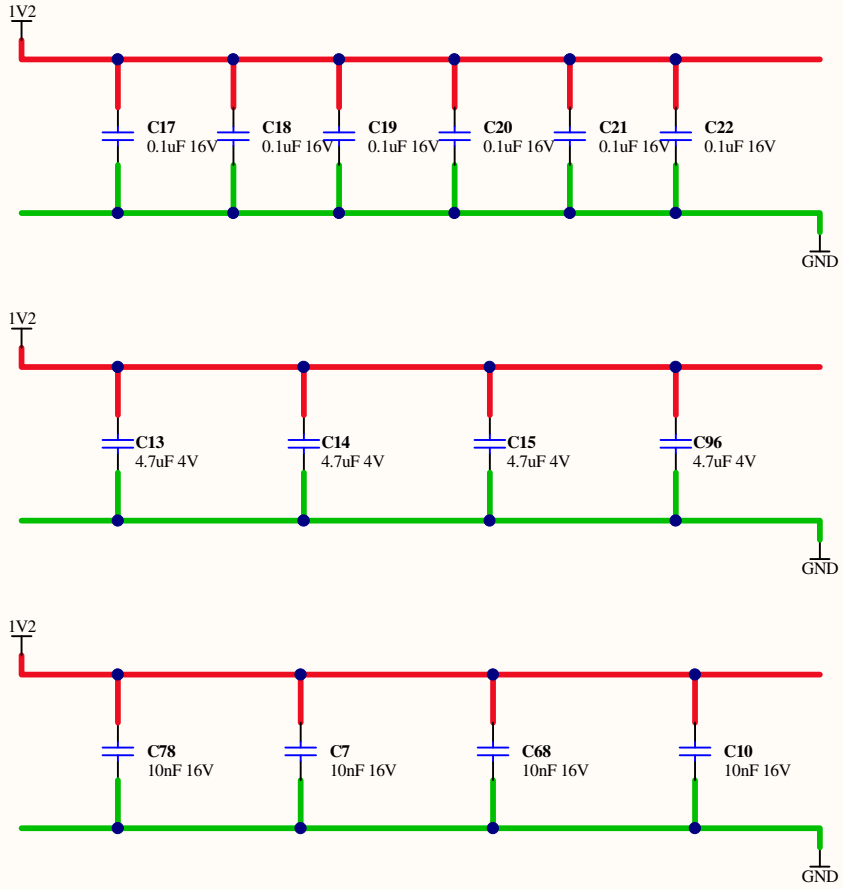
SOM PIN DESCRIPTIONS:

SERVICES:

- 18x 4.5V TO 5.5V POWER PINS (5.4AMPS)
- 140x SINGLE ENDED 3.3V IO
- 13x DIFFERENTIAL PAIRS
- 11x SINGLE ENDED GLOBAL CLOCKS
- 1x DIFFERENTIAL GLOBAL CLOCK
- 4x 5VDC 600mA POWER OUTPUTS (ie USB PORT POWER)
- 2x 3.3VDC 600mA POWER OUTPUTS (ie SDCARD POWER)
- PLUG PACK DETECT/MONITOR (PMBUS)
- SOM ID ROM (SOM ID)
- HARD JTAG WITH ADAPTIVE CLOCKING OPTION
- SOM JTAG CONTROLLER DETECT AND BUS REQUEST (JTAG SEL)

POWER HANDLING CAPACITY
MAX VOLTAGE PER PIN: 25V
MAX CURRENT PER PIN: 0.3A
NUMBER OF POWER PINS: GND x 19/+B x 18
MAX MODULE POWER: 27W (5V @ 5.4A)

Title		
Size: A2	Number	Revision
Date: 23/09/2011		Sheet of
File: C:\SRKH\..\FPGA_SOM_IO.SchDoc		Drawn By:



Sheet Title	*FPGA Bypass 2V5*		
Project Title	*SOM02*		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 3 of 13	
File: FPGA_Bypass_FPGA_1V2.SchDoc			

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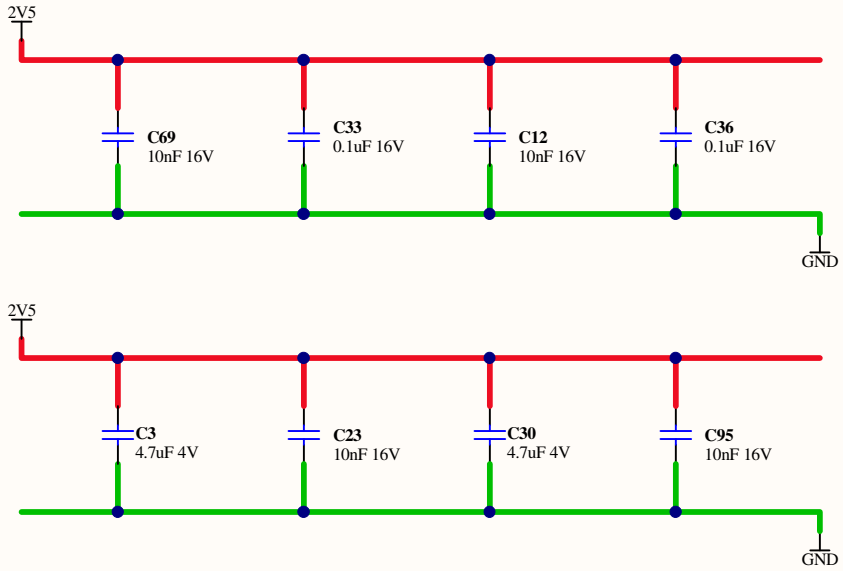

Sheet Title	***FPGA Bypass 2V5***		
Project Title	***SOM02***		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 4 of 13	
File: FPGA_Bypass_FPGA_2V5.SchDoc			

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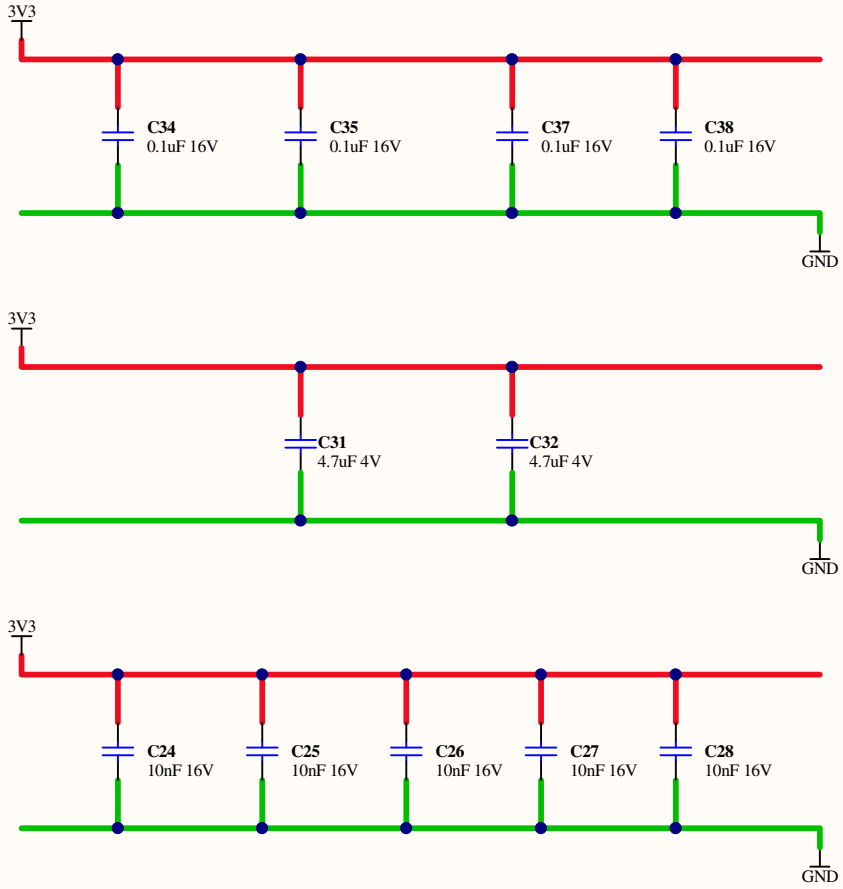

Sheet Title	***FPGA Bypass 2V5***		
Project Title	***SOM02***		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 5 of 13	
File: FPGA_Bypass_FPGA_3V3.SchDoc			

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SRAM - 64K/256K x 16

SRAM-256Kx16

SRAM

A[18..0] D[15..0] NCS NWE NOE NBHE NBLE

SRAM_A[18..0] SRAM_D[15..0] SRAM_NCS SRAM_NWE SRAM_NOE SRAM_NBHE SRAM_NBLE

IO — IO — FPGA_IO[140..1] — FPGA_IO[140..1]

SYSCLK — SYSCLK — 24MHZ

WAKE/SLEEP

PWR_STATUS — ON_REQ PM_BUS — ON_REQ PM_BUS

HARDSOFT_JTAG

JTAG — HARD: TDI TMS TCK TDO — HARD_TDI HARD_TMS HARD_TCK HARD_TDO

SOFT: TMS TCK TDI TDO — SOFT_TMS SOFT_TCK SOFT_TDI SOFT_TDO

JTAG_RCLK JTAG_SEL — HARD_RTCK JTAG_SEL

R2 5R6 1%

FPGA_NonIO — FPGA_NonIO.SchDoc

TDI TMS TCK TDO FBTCK

GCLK0
FPGA SYSTEM CLOCK IS ON GLOBAL CLOCK 0
24MHZ

1V2

FPGA_DECOUPLING_CAPS_1V2
FPGA_Bypass_FPGA_1V2.SchDoc

2V5

FPGA_DECOUPLING_CAPS_2V5
FPGA_Bypass_FPGA_2V5.SchDoc

3V3

FPGA_DECOUPLING_CAPS_3V3
FPGA_Bypass_FPGA_3V3.SchDoc

PWR_CTRL[6..1] — PWR_CTRL — PWR_CTRL[6..1] — PWR_CTRL

XILINX MULTIBOOT COMPATIBLE
GOLDEN

SERFLASH — SERFLASH — FLASH_CS_N DOUT DIN SCLK — FLASH_GOLD_CS_N FLASH_GOLD_DOUT FLASH_GOLD_DIN FLASH_GOLD_CLK

FPGA WILL ATTEMPT SPI BOOT THREE TIMES (UG332-P227)

NOTE:
INIT_B ASSERTS DURING CONFIG.
DOUT OSCILLATES DURING CONFIG.

U3A — XC3S1600E-4FGG400C — BANK 0

IO_L01P_0	C17	SRAM_D14
IO_L01N_0	D17	SRAM_D7
IO_L03P_0	A19	SRAM_D3
IO_L03N_0/VREF_0	A18	SRAM_D5
IO	E16	SRAM_NBLE
IO_L04P_0	A16	SRAM_D15
IO_L04N_0	A17	SRAM_D13
IO_L06P_0	B15	SRAM_D2
IO_L06N_0	A15	SRAM_NOE
IO	E14	JTAG_SEL
IO_L07P_0	D14	SRAM_D6
IO_L07N_0	C14	SRAM_D4
IO_L09P_0	A14	SRAM_D12
IO_L09N_0/VREF_0	A13	SRAM_A7
IO	E13	FPGA_IO15
IO_L10P_0	C13	SRAM_A6
IO_L10N_0	B13	SRAM_NWE
IO	E13	SRAM_A5
IO_L12P_0	D12	SOFT_TMS
IO_L12N_0	C12	SRAM_D11
IO	A12	SRAM_D10
IO_L13P_0	C12	FPGA_IO1
IO_L13N_0	B12	FPGA_IO2
IO_L15P_0/GCLK4	C11	FPGA_IO26
IO_L15N_0/GCLK5	D11	FPGA_IO28
IO/VREF_0	C11	SRAM_D9
IO_L16P_0/GCLK6	E11	FPGA_IO34
IO_L16N_0/GCLK7	E10	FPGA_IO37
IO_L18P_0/GCLK10	A9	FPGA_IO36
IO_L18N_0/GCLK11	C10	IONC30
IO	B9	FPGA_IO7
IO_L19P_0	B9	FPGA_IO8
IO_L19N_0	D9	FPGA_IO19
IO_L21P_0	B9	SRAM_A18
IO_L21N_0	A8	SRAM_A8
IO	B9	FPGA_IO5
IO_L22P_0	D8	FPGA_IO6
IO_L22N_0/VREF_0	D8	SRAM_A13
IO	A8	FPGA_IO3
IO_L24P_0	C7	FPGA_IO4
IO_L24N_0/VREF_0	C7	SRAM_A9
IO	A7	FPGA_IO11
IO_L25P_0	A6	FPGA_IO12
IO_L25N_0	B6	FPGA_IO16
IO_L27P_0	B5	FPGA_IO17
IO_L27N_0	C7	SRAM_A14
IO	C6	FPGA_IO9
IO_L28P_0	D6	FPGA_IO10
IO_L28N_0	C5	SOFT_TDO
IO_L30P_0	C5	SRAM_A11
IO_L30N_0/VREF_0	A3	FPGA_IO21
IO	B2	FPGA_IO13
IO_L31P_0	C5	SRAM_A12
IO_L31N_0	A2	FPGA_IO14
IO_L32P_0	C4	SOFT_TDI
IO_L32N_0/HSWAP	D4 (OUTPUT ONLY)	SRAM_A12

R21 1K 1%

GND

HSWAP (INT PULLED UP VIA FIXED RESISTOR)
HSWAP HIGH = INT PULLUPS OFF
HSWAP LOW= INT PULLUPS ON
(DS312-P72)

[HSWAP]
HSWAP = L
EXTERNAL PULL DOWN
TO ENABLE PULL UP RESISTORS
ON ALL IO

INTERNAL XC3SxxxE RESISTANCE VALUES
RPU - PULL UP RESISTOR (VCCO = 3V3) = 10K8 OHMS
RPD - PULL DOWN RESISTOR (VCCO = 3V3) = 54K5 OHMS

U3B — XC3S1600E-4FGG400C — BANK 1

IO_L01P_1/A16	U17	PWR_CTRL4
IO_L01N_1/A15	T17	FPGA_IO59
IO_L02P_1/A14	T17	IONC0
IO_L02N_1/A13	T18	FPGA_IO60
IO_L03P_1	T19	FPGA_IO62
IO_L03N_1/VREF_1	T19	FPGA_IO114
IO_L04P_1	V20	ON_REQ
IO_L04N_1	W20	FPGA_IO110
IO_L05P_1	R17	IONC2
IO_L05N_1	R18	FPGA_IO112
IO_L06P_1	U20	PM_BUS
IO_L06N_1	P20	IONC3
IO_L07P_1	P17	IONC4
IO_L07N_1	P18	PWR_CTRL5
IO_L08P_1	R20	FPGA_IO101
IO_L08N_1/VREF_1	P20	FPGA_IO117
IO_L09P_1	N16	FPGA_IO109
IO_L09N_1	P16	FPGA_IO107
IO_L10P_1	N18	IONC6
IO_L10N_1	N19	IONC7
IO_L11P_1	M15	FPGA_IO83
IO_L11N_1	M15	IONC5
IO_L12P_1/A12	M17	FPGA_IO108
IO_L12N_1/A11	M18	FPGA_IO111
IO_L13P_1	M19	IONC8
IO_L13N_1/VREF_1	L19	FPGA_IO67
IO_L14P_1/A10/RHCLK0	M16	FPGA_IO115
IO_L14N_1/A9/RHCLK1	N17	IONC9
IO_L15P_1/A8/RHCLK2	L17	IONC10
IO_L15N_1/A7/RHCLK3/TRDY1	L14	IONC11
IO_L16P_1/A6/RHCLK4/IRDY1	K13	IONC12
IO_L16N_1/A5/RHCLK5	K14	IONC13
IO_L17P_1/A4/RHCLK6	K20	FPGA_IO18
IO_L17N_1/A3/RHCLK7	J20	IONC15
IO_L18P_1/A2	J16	SRAM_A15
IO_L18N_1/A1	J16	FPGA_IO20
IO_L19P_1	J14	IONC17
IO_L19N_1/A0	L3	IONC18
IO_L20P_1	J18	SRAM_D8
IO_L20N_1	J19	IONC16
IO_L21P_1	J19	IONC20
IO_L21N_1	H16	IONC23
IO_L22P_1	H15	IONC14
IO_L22N_1	H17	IONC21
IO_L23P_1	H18	IONC22
IO_L23N_1	E20	SRAM_NBHE
IO_L24P_1	E20	SRAM_D1
IO_L24N_1/VREF_1	E16	FPGA_IO33
IO_L25P_1	E16	IONC24
IO_L25N_1	D20	SRAM_A0
IO_L26P_1	D19	SRAM_A16
IO_L26N_1	E17	IONC1
IO_L27P_1	E18	SRAM_NCS
IO_L27N_1	E20	SRAM_D0
IO_L28P_1	D20	SRAM_A1
IO_L28N_1	D18	SRAM_A2
IO_L29P_1/HDC	D18	SRAM_A17
IO_L29N_1/LDC0	C20	SRAM_A4
IO_L30P_1/LDC1	W2	SRAM_A3
IO_L30N_1/LDC2	T19	

R2 5R6 1%

U3C — XC3S1600E-4FGG400C — BANK 2

IO_L01P_2/CSO_B	U4	FLASH_GOLD_CS_N
IO_L01N_2/INIT_B	V4	FPGA_IO91
IO_L03P_2/DOUT/BUSY	U5 (OUTPUT ONLY)	IONC25
IO_L03N_2/MOSI/CSI_B	V5	FLASH_GOLD_DIN
IO/VREF_2	T3	FPGA_IO89
IO_L04P_2	W4	FPGA_IO120
IO_L04N_2	Y4	FPGA_IO93
IO_L06P_2	V5	FPGA_IO122
IO_L06N_2	U6	PWR_CTRL6
IO	Y5	FPGA_IO123
IO_L07P_2	V7	FPGA_IO124
IO_L07N_2	U7	FPGA_IO126
IO_L09P_2	R7	FPGA_IO96
IO_L09N_2/VREF_2	R7	FPGA_IO92
IO	Y7	FPGA_IO99
IO_L10P_2	W8	FPGA_IO95
IO_L10N_2	V8	FPGA_IO125
IO	R8	FPGA_IO97
IO_L12P_2	V9	FPGA_IO79
IO_L12N_2	R9	FPGA_IO129
IO	R9	FPGA_IO127
IO_L13P_2	Y9	FPGA_IO98
IO_L13N_2	R8	IONC26
IO_L15P_2/D7/GCLK12	W9	FPGA_IO139
IO_L15N_2/D6/GCLK13	W10	FPGA_IO140
IO/D5	N11	FPGA_IO100
IO_L16P_2/D4/GCLK14	R10	FPGA_IO121
IO_L16N_2/D3/GCLK15	P10	FPGA_IO113
IO_L18P_2/D2/GCLK2	T10	FPGA_IO87
IO_L18N_2/D1/GCLK3	V11	FPGA_IO103
IO/M1	F11	HOST_M1
IO_L19P_2/M0	F11	HOST_M0
IO_L19N_2/DIN/D0	T12	FLASH_GOLD_DOUT
IO_L21P_2	V12	FPGA_IO137
IO_L21N_2	U12	FPGA_IO138
IO	W13	IONC27
IO_L22P_2	W12	PWR_CTRL6
IO_L22N_2/VREF_2	W12	PWR_CTRL2
IO	R13	FPGA_IO104
IO_L24P_2	V13	FPGA_IO131
IO_L24N_2	U13	FPGA_IO132
IO	T13	FPGA_IO105
IO_L25P_2	R14	FPGA_IO106
IO_L25N_2	U14	IONC28
IO_L27P_2/A23	V15	FPGA_IO135
IO_L27N_2/A22	T14	FPGA_IO136
IO	W15	PWR_CTRL3
IO_L28P_2	U15	FPGA_IO133
IO_L28N_2	T15	FPGA_IO134
IO_L30P_2/A21	U16	FPGA_IO130
IO_L30N_2/A20	V16	FPGA_IO103
IO/VREF_2	Y17	IONC19
IO_L31P_2/VS2/A19	W18	HOST_VS0
IO_L31N_2/VS1/A18	R18	HOST_VS1
IO_L32P_2/VS0/A17	Y19	HOST_VS2
IO_L32N_2/CCLK	W19	FLASH_GOLD_CLK

U3D — XC3S1600E-4FGG400C — BANK 3

IO_L01P_3	D3	FPGA_IO24
IO_L01N_3	E2	FPGA_IO29
IO_L02P_3	E3	SRAM_A10
IO_L02N_3/VREF_3	E1	FPGA_IO25
IO_L03P_3	D1	FPGA_IO23
IO_L03N_3	D1	FPGA_IO27
IO_L04P_3	E1	FPGA_IO31
IO_L04N_3	F4	FPGA_IO38
IO_L05P_3	F3	FPGA_IO32
IO_L05N_3	F2	FPGA_IO35
IO_L06P_3	F1	FPGA_IO39
IO_L06N_3	G3	FPGA_IO60
IO_L07P_3	G4	FPGA_IO40
IO_L07N_3	F5	FPGA_IO63
IO_L08P_3	G5	FPGA_IO41
IO_L08N_3	E5	FPGA_IO61
IO_L09P_3	H3	FPGA_IO42
IO_L09N_3/VREF_3	H5	FPGA_IO62
IO_L10P_3	H7	IONC29
IO_L10N_3	F1	FPGA_IO45
IO_L11P_3	H4	FPGA_IO43
IO_L11N_3	H2	FPGA_IO47
IO_L12P_3	J1	FPGA_IO66
IO_L12N_3	G6	FPGA_IO65
IO_L13P_3	J5	FPGA_IO44
IO_L13N_3	K3	FPGA_IO49
IO_L14P_3/LHCLK0	K2	FPGA_IO68
IO_L14N_3/LHCLK1	K1	FPGA_IO64
IO_L15P_3/LHCLK2	K7	FPGA_IO67
IO_L15N_3/LHCLK3/IRDY2	M1	FPGA_IO69
IO_L16P_3/LHCLK4/TRDY2	L4	FPGA_IO48
IO_L16N_3/LHCLK5	M3	FPGA_IO52
IO_L17P_3/LHCLK6	L3	FPGA_IO70
IO_L17N_3/LHCLK7	M8	FPGA_IO76
IO_L18P_3	M6	FPGA_IO51
IO_L18N_3	M5	FPGA_IO71
IO_L19P_3	M4	FPGA_IO50
IO_L19N_3	M6	FPGA_IO73
IO_L20P_3	N6	FPGA_IO57
IO_L20N_3/VREF_3	N1	FPGA_IO72
IO_L21P_3	N2	FPGA_IO54
IO_L21N_3	N7	FPGA_IO119
IO_L22P_3	P7	FPGA_IO84
IO_L22N_3/VREF_3	N3	FPGA_IO74
IO_L23P_3	P3	FPGA_IO55
IO_L23N_3	P1	FPGA_IO53
IO_L24P_3	R1	FPGA_IO75
IO_L24N_3	P5	FPGA_IO94
IO_L25P_3	R5	FPGA_IO81
IO_L25N_3	R2	FPGA_IO78
IO_L26P_3	T2	FPGA_IO118
IO_L26N_3	R3	FPGA_IO58
IO_L27P_3	R4	FPGA_IO56
IO_L27N_3	U1	FPGA_IO85
IO_L28P_3	T1	FPGA_IO77
IO_L28N_3/VREF_3	T3	FPGA_IO86
IO_L29P_3	T3	FPGA_IO116
IO_L29N_3	T2	FPGA_IO88
IO_L30P_3	V1	FPGA_IO90
IO_L30N_3	T4	

U3E — XC3S1600E-4FGG400C

IP_L29N_0	A4	INC0
IP_L29P_0	A5	INC1
IP_L26N_0	B6	INC2
IP_L26P_0	E7	INC3
IP_L23N_0	F8	INC4
IP_L23P_0	D8	INC5
IP_L20N_0	G9	INC6
IP_L20P_0	G8	INC7
IP_L17N_0/GCLK9	G10	INC8
IP_L17P_0/GCLK8	H10	24MHZ
IP_L14N_0	B11	INC10
IP_L14P_0	B12	INC11
IP_L11N_0	G14	INC12
IP_L11P_0	G13	INC13
IP_L08N_0	E14	INC14
IP_L08P_0	E15	INC15
IP_L05N_0	D15	INC16
IP_L05P_0	C15	INC17
IP_L02N_0	E16	INC18
IP_L02P_0	D16	INC19
IP	B18	INC20
IP	E5	INC21
IP	G18	INC22
IP	B20	INC23
IP	E19	INC24
IP/VREF_1	G15	INC25
IP	H14	INC26
IP	H15	INC27
IP	K18	INC28
IP/VREF_1	L18	INC29
IP	K19	INC30
IP	K20	INC31
IP	N14	INC32
IP	P15	INC33
IP	R19	INC34
IP	R16	INC35
IP	T16	INC36
IP_L29N_2	W16	INC37
IP_L29P_2	V16	INC38
IP_L26N_2	V14	INC39
IP_L26P_2	U15	INC40
IP_L23N_2/VREF_2	T13	INC41
IP_L23P_2	T14	INC42
IP_L20N_2	U12	INC43
IP_L20P_2	R12	INC44
IP_L17N_2/M2/GCLK1	P12	HOST_M2
IP_L17P_2/RDWR_B/GCLK0	P11	SOFT_TCK
IP_L14N_2/VREF_2	T10	INC45
IP_L14P_2	T9	INC46
IP_L11N_2	R8	INC47
IP_L11P_2	T8	INC48
IP_L08N_2	V6	INC49
IP_L08P_2	W6	INC50
IP_L05N_2	V6	INC51
IP_L05P_2	U6	INC52
IP_L02N_2	V2	INC53
IP_L02P_2	W2	INC54
IP	V3	INC55
IP	T4	INC56
IP	W1	INC57
IP/VREF_3	P6	INC58
IP	N5	INC59
IP	P3	INC60
IP	M2	INC61
IP	L5	INC62
IP	L8	INC63
IP/VREF_3	L6	INC64
IP	J5	INC65
IP	H1	INC66
IP	G1	INC67
IP	G6	INC68
IP	F5	INC69

M0, M1, M2
SET EXTERNAL SPI MASTER
BOOT FROM EXTERNAL SPI FLASH

M0 = H
EXTERNAL PULL UP
M1 = L
EXTERNAL PULL DOWN
M2 = L
EXTERNAL PULL DOWN
(UG332-P34)

XC3S1600E MODE PIN CONFIGURATIONS

M2_M1_M0	FUNCTION:
0 0 0	PLATFORM FLASH MODE
0 0 1	SPI MODE (MASTER)
0 1 0	BYTE PARALLEL INTERFACE
0 1 1	INTERNAL MASTER SPI FLASH
1 0 0	<RESERVED>
1 0 1	JTAG MODE
1 1 0	SLAVE PARALLEL
1 1 1	SLAVE SERIAL

XC3S1600E SPI MODE CONFIGURATIONS

VS2_VS1_VS0	FUNCTION:
0 0 0	<RESERVED>
0 0 1	<RESERVED>
0 1 0	<RESERVED>
0 1 1	<RESERVED>
1 0 0	<RESERVED>
1 0 1	(0x03) STANDARD READ
1 1 0	(0xE8) READ ARRAY
1 1 1	(0xBB) SPI FAST READ

M0 (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
EXT SPI BOOT MODE (MASTER)

M1 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
EXT SPI BOOT MODE (MASTER)

M2 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
EXT SPI BOOT MODE (MASTER)

VS0 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO_2

VS1 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO_2

VS2 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO_2

[M0]
M0 = H
INTERNAL PULL UP
BY HSWAP PRIOR TO
CONFIGURATION
(UG332-P47)
(UG332-P98)

SPI MODE (MASTER)
HOST_M0 — [M0] — R10 2K2 1% — 3V3

HOST_M1 — [M1] — R9 100R 1% — GND

HOST_M2 — [M2] — R8 100R 1% — GND

(0x0B) SPI FAST READ
HOST_VS0 — R7 2K2 1% — 3V3

HOST_VS1 — R6 2K2 1% — 3V3

HOST_VS2 — R5 2K2 1% — 3V3

[VS0, VS1, VS2]
VSx = H
INTERNAL PULL UP BY
HSWAP PRIOR TO CONFIG
VS = FAST READ (0x0B)
(UG332-P100)
(DS312-P79)
(UG332-P98)

Sheet Title	Host Controller - Spartan3AN-400		
Project Title	SOM02		
Size: A2	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 6 of 13	
File: FPGA.SchDoc			

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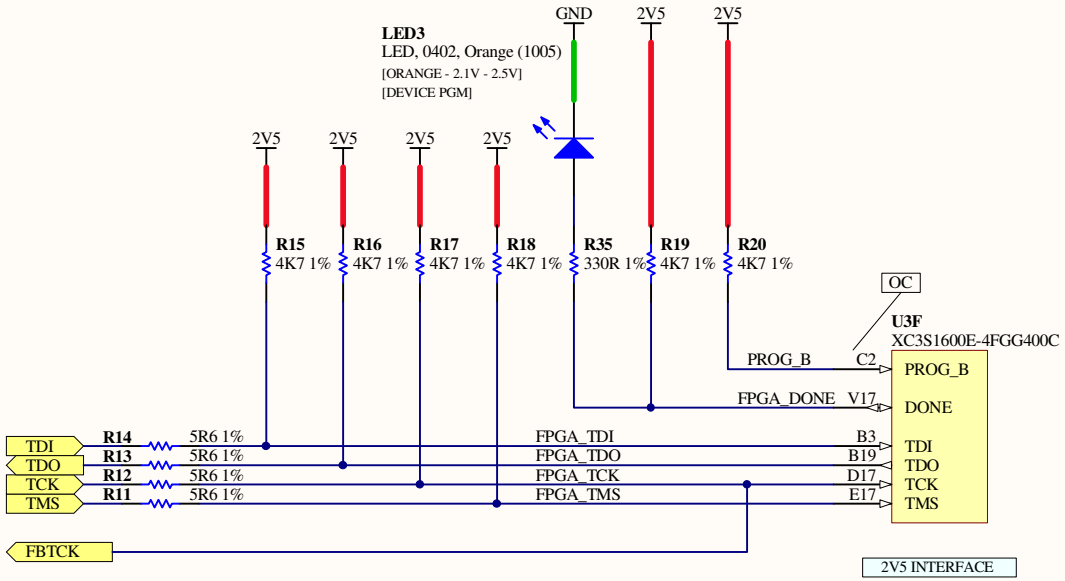
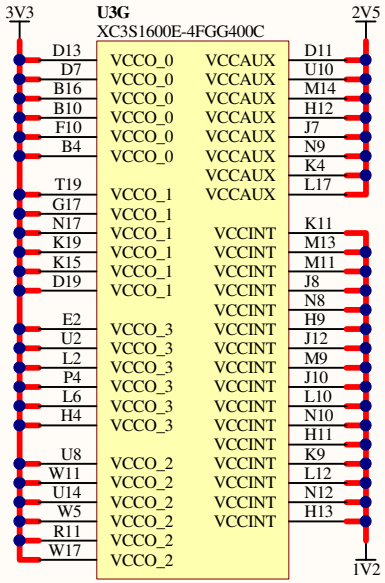


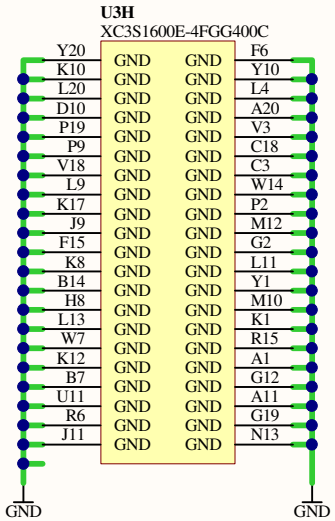
TDI, TDO, TCK AND TMS ALL REQUIRE SERIES RESISTOR FOR 3.3V OPERATION
(XAPP453-P13)

PROG_B (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
TO ALLOW CONFIGURATION TO START

DONE (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
HIGH = PROGRAM SUCCESSFUL

FPGA_DONE PIN
H = PROGRAMMED (LOADED)
INTERNAL PULL UP
LOW BY DEFAULT





Sheet Title	*HOST FPGA Pwr and Programming*		
Project Title	*SOM02*		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 7 of 13	
File: FPGA_NonIO.SchDoc			

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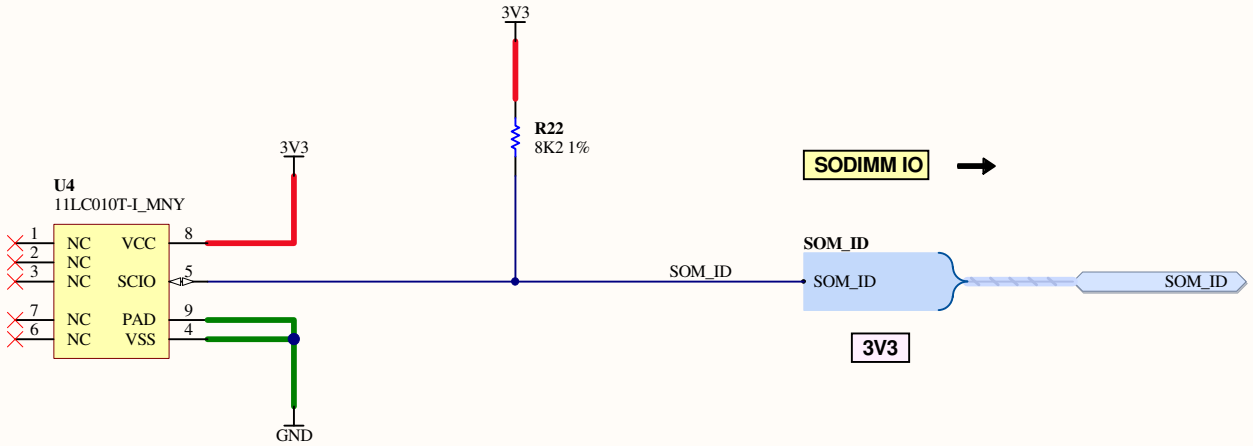
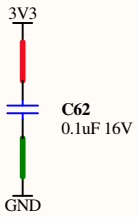
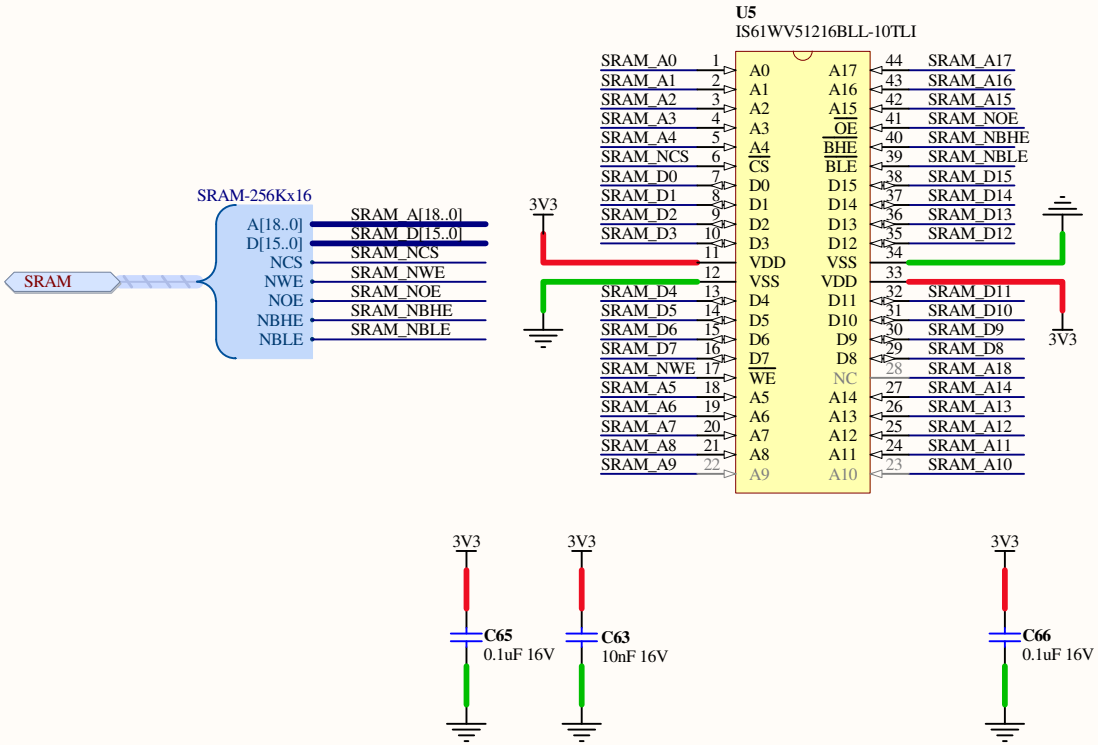




11LC010T-I_MNY POWER CONSUMPTION

STANDBY:	3V3	1uA
ACTIVE:	3V3	1mA

Title		
Size: A4	Number	Revision
Date: 23/09/2011	Sheet of	
File: C:\SRKH\SOM03 - XC3S1600E\SOM_ID.SchDoc	Drawn By:	



DEFAULT

IS61WV25616BLS FAST SRAM *(10nS)*
256K x16 BITS **512K bytes**

IS61WV51216BLL-10TLI FAST SRAM *(10nS)*
512K x16 BITS **1M bytes**

IS61WV20488BLL-10TLI FAST SRAM *(10nS)*
2048K x8 BITS **2M bytes**

Sheet Title	***256K x 16-Bit SRAM***		
Project Title	***SOM02***		
Size: A4	Assy: TBA	Revision: 04	
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File: SRAM_512Kx16_TSOP44.SchDoc			

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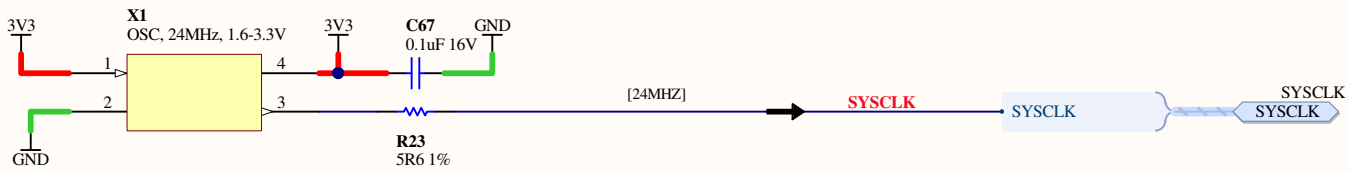

Sheet Title	*16M x 32 SDRAM TSOP54 x 2*		
Project Title	*SOM02*		
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011 Time: 1:27:40 PM		Sheet 10 of 13	
File: SYS_CLK.SchDoc			

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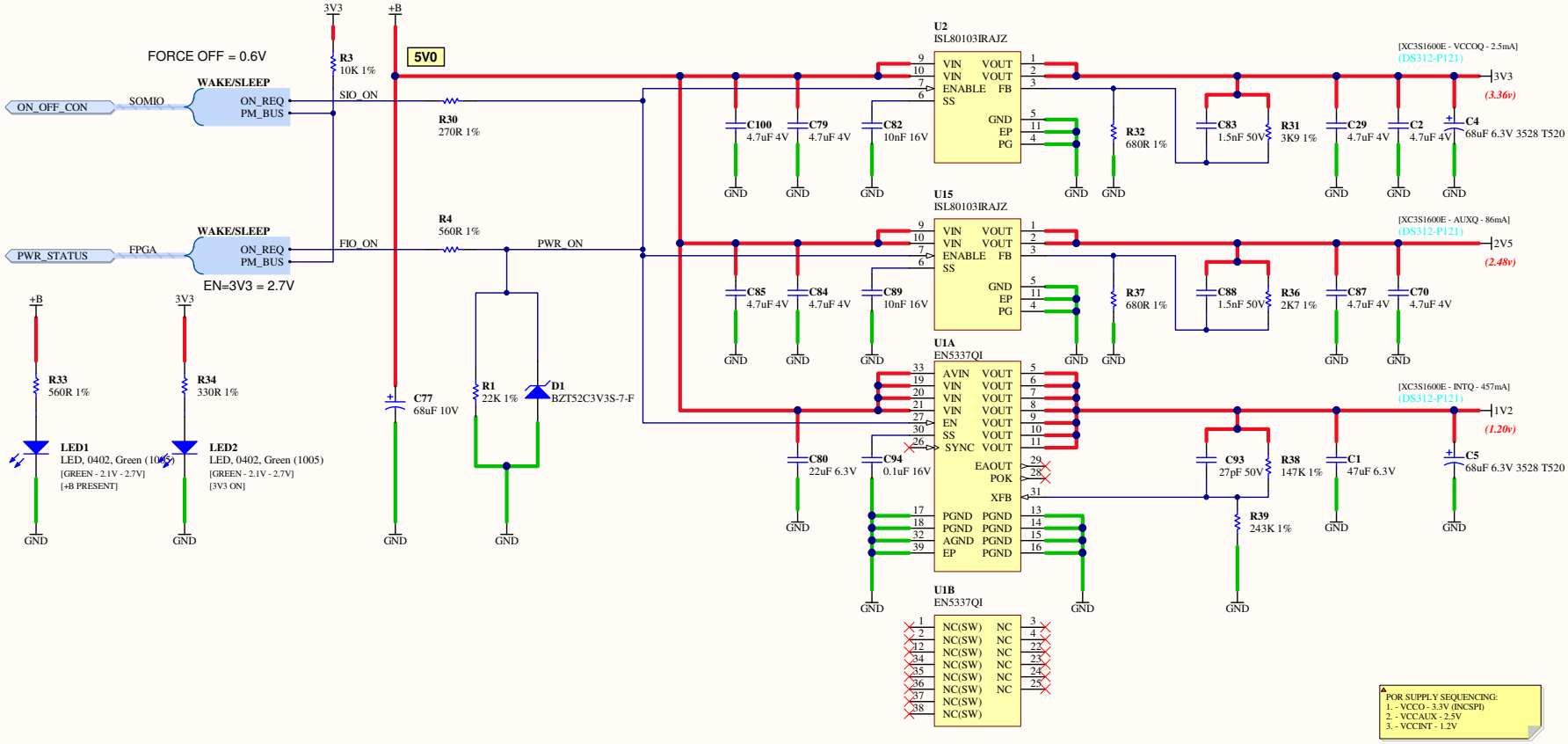
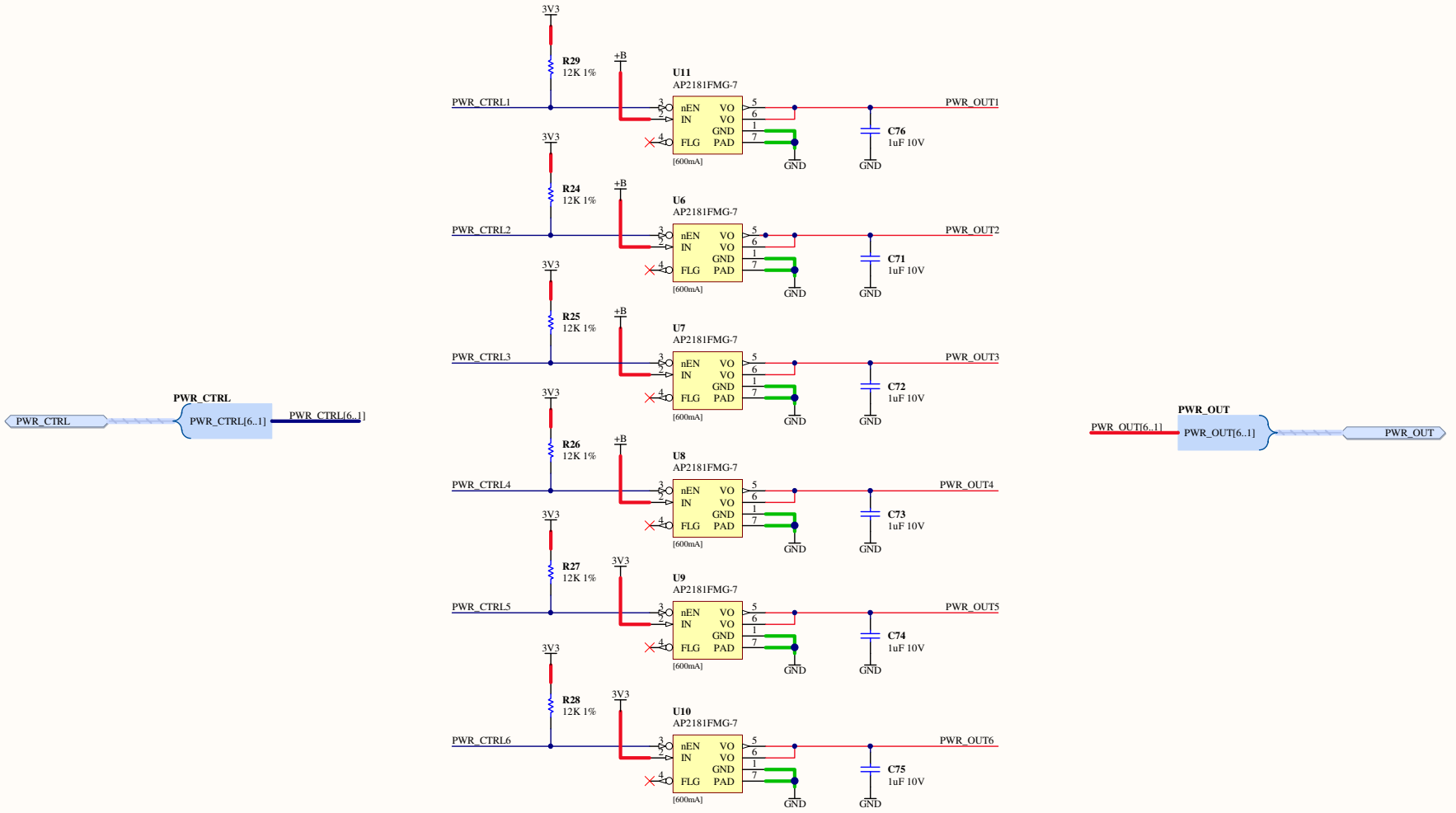
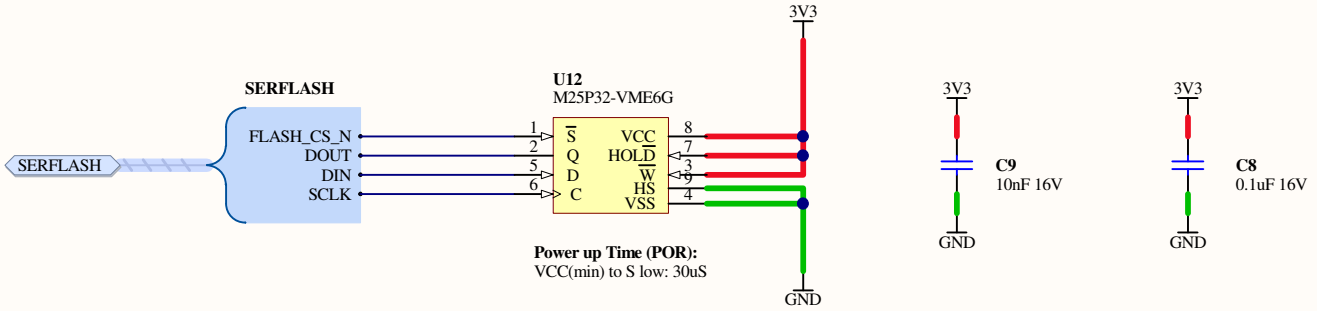

FORCE OFF = 0.6V
WAKE/SLEEP
ON_OFF_CON
SOMIO
ON_REQ
PM_BUS
SIO_ON
R3
10K 1%
3V3
+B
5V0
R30
270R 1%
WAKE/SLEEP
PWR_STATUS
FPGA
ON_REQ
PM_BUS
FIO_ON
R4
560R 1%
PWR_ON
EN=3V3 = 2.7V
R33
560R 1%
LED1
LED, 0402, Green (1005)
[GREEN - 2.1V - 2.7V]
[+B PRESENT]
R34
330R 1%
LED2
LED, 0402, Green (1005)
[GREEN - 2.1V - 2.7V]
[3V3 ON]
C77
68uF 10V
R1
22K 1%
D1
BZT52C3V3S-7-F
GND
U2
ISL80103IRAJZ
VIN
VOUT
ENABLE
FB
SS
GND
EP
PG
C100
4.7uF 4V
C79
4.7uF 4V
C82
10nF 16V
R32
680R 1%
C83
1.5nF 50V
R31
3K9 1%
C29
4.7uF 4V
C2
4.7uF 4V
C4
68uF 6.3V 3528 T520
[XC3S1600E - VCCOQ - 2.5mA]
(DS312-P121)
3V3
(3.36v)
U15
ISL80103IRAJZ
C85
4.7uF 4V
C84
4.7uF 4V
C89
10nF 16V
R37
680R 1%
C88
1.5nF 50V
R36
2K7 1%
C87
4.7uF 4V
C70
4.7uF 4V
[XC3S1600E - AUXQ - 86mA]
(DS312-P121)
2V5
(2.48v)
U1A
EN5337QI
AVIN
VOUT
VIN
EN
SS
SYNC
EAOUT
POK
XFB
PGND
AGND
EP
C80
22uF 6.3V
C94
0.1uF 16V
C93
27pF 50V
R38
147K 1%
C1
47uF 6.3V
C5
68uF 6.3V 3528 T520
[XC3S1600E - INTQ - 457mA]
(DS312-P121)
1V2
(1.20v)
R39
243K 1%
U1B
EN5337QI
NC(SW)
NC
POR SUPPLY SEQUENCING:
1. - VCCO - 3.3V (INCSPI)
2. - VCCAUX - 2.5V
3. - VCCINT - 1.2V


PWR_CTRL
PWR_CTRL
PWR_CTRL[6..1]
PWR_CTRL[6..1]
3V3
+B
R29
12K 1%
U11
AP2181FMG-7
PWR_CTRL1
nEN
IN
FLG
VO
VO
GND
PAD
[600mA]
PWR_OUT1
C76
1uF 10V
GND
R24
12K 1%
U6
AP2181FMG-7
PWR_CTRL2
PWR_OUT2
C71
1uF 10V
R25
12K 1%
U7
AP2181FMG-7
PWR_CTRL3
PWR_OUT3
C72
1uF 10V
R26
12K 1%
U8
AP2181FMG-7
PWR_CTRL4
PWR_OUT4
C73
1uF 10V
R27
12K 1%
U9
AP2181FMG-7
PWR_CTRL5
PWR_OUT5
C74
1uF 10V
R28
12K 1%
U10
AP2181FMG-7
PWR_CTRL6
PWR_OUT6
C75
1uF 10V
PWR_OUT
PWR_OUT[6..1]
PWR_OUT[6..1]
PWR_OUT



DEFAULT

M25P32-VME6G 32Mbit Serial PROM *(75MHz)*
33,554,432 BITS **4M bytes**
(ID=0x2016)

M25P64-VME6G 64Mbit Serial PROM *(75MHz)*
67,108,864 BITS **8M bytes**
(ID=0x2017)

M25P128-VME6G 128Mbit Serial PROM *(54MHz)*
134,217,728 BITS **16M bytes**
(ID=0x2018)

W25Q256FV 256Mbit Serial PROM *(80MHz)*
268,435,456 BITS **32M bytes**
(ID=0x4019)

Sheet Title: ***Host - Dual Serial Flash Memory***		
Project Title: ***SOM02***		
Size: A4	Assy: TBA	Revision: 04
Date: 23/09/2011 Time: 1:27:40 PM		Sheet 13 of 13
File: FLASH_M25P_SPI.SchDoc		

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