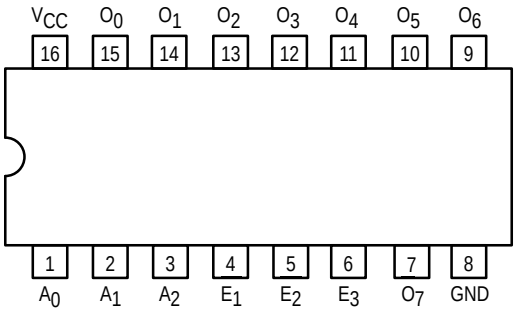
MOTOROLA

# 1-OF-8 DECODER/ DEMULTIPLEXER

The LSTTL/MSI SN54/74LS138 is a high speed 1-of-8 Decoder/ Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Typical Power Dissipation of 32 mW
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

**CONNECTION DIAGRAM DIP** (TOP VIEW)



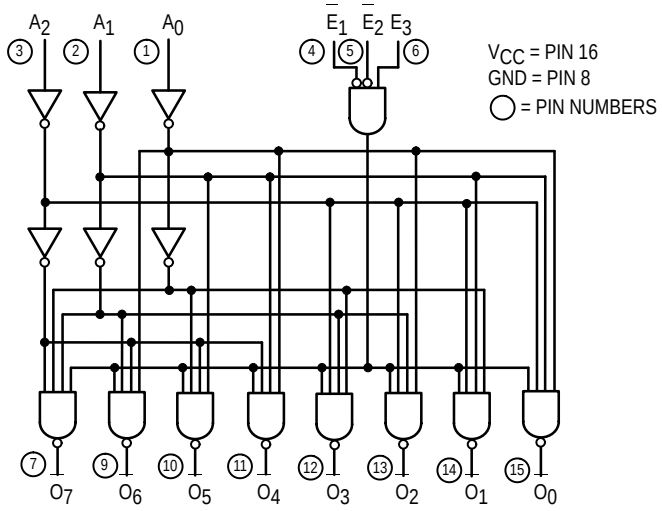

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

**PIN NAMES**

| | | **LOADING** (Note a) | |
|---|---|---|---|
| | | HIGH | LOW |
| $\underline{A}_0 - \underline{A}_2$ | Address Inputs | 0.5 U.L. | 0.25 U.L. |
| $E_1$, $E_2$ | Enable (Active LOW) Inputs | 0.5 U.L. | 0.25 U.L. |
| $\underline{E}_3$ | Enable (Active HIGH) Input | 0.5 U.L. | 0.25 U.L. |
| $O_0 - O_7$ | Active LOW Outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

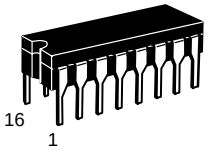
**LOGIC DIAGRAM**



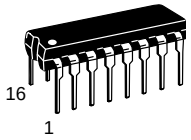

# SN54/74LS138

**1-OF-8 DECODER/ DEMULTIPLEXER**

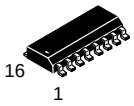
**LOW POWER SCHOTTKY**




**J SUFFIX**
CERAMIC
CASE 620-09




**N SUFFIX**
PLASTIC
CASE 648-08

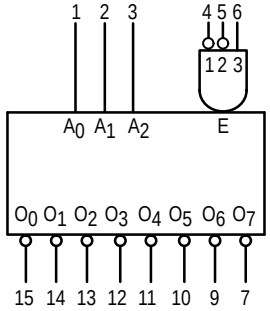



**D SUFFIX**
SOIC
CASE 751B-03

**ORDERING INFORMATION**

| | |
|---|---|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC |

**LOGIC SYMBOL**




VCC = PIN 16
GND = PIN 8

## FUNCTIONAL DESCRIPTION

The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs ($A_0$, $A_1$, $A_2$) and when enabled provides eight mutually exclusive active LOW Outputs ($\overline{O_0}$–$\overline{O_7}$). The LS138 features three Enable inputs, two active LOW ($\overline{E_1}$, $\overline{E_2}$) and one active HIGH ($E_3$). All outputs will be HIGH unless $\overline{E_1}$ and $\overline{E_2}$ are LOW and $E_3$ is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

**TRUTH TABLE**

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E_1}$ | $\overline{E_2}$ | $E_3$ | $A_0$ | $A_1$ | $A_2$ | $\overline{O_0}$ | $\overline{O_1}$ | $\overline{O_2}$ | $\overline{O_3}$ | $\overline{O_4}$ | $\overline{O_5}$ | $\overline{O_6}$ | $\overline{O_7}$ |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | H | L | L | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | H | L | H | H | H | L | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | L | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

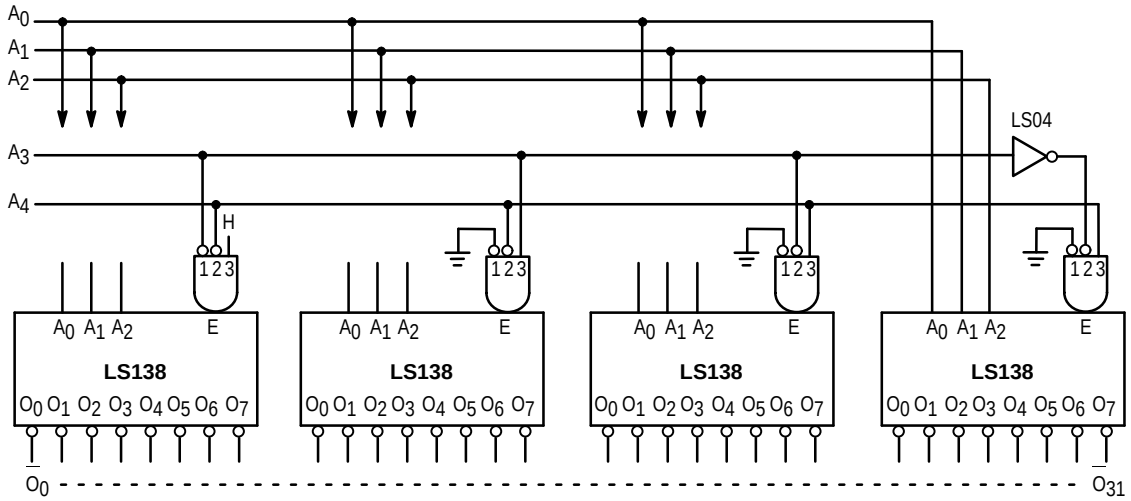



**Figure a**

## GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 54<br>74 | –55<br>0 | 25<br>25 | 125<br>70 | °C |
| $I_{OH}$ | Output Current — High | 54, 74 | | | –0.4 | mA |
| $I_{OL}$ | Output Current — Low | 54<br>74 | | | 4.0<br>8.0 | mA |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | | Limits Min | Limits Typ | Limits Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | –0.65 | –1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = –18 mA | |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | |
| | | 74 | 2.7 | 3.5 | | V | | |
| $V_{OL}$ | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{IH}$ | Input HIGH Current | | | | 20 | µA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | |
| | | | | | 0.1 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| $I_{IL}$ | Input LOW Current | | | | –0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| $I_{OS}$ | Short Circuit Current (Note 1) | | –20 | | –100 | mA | $V_{CC}$ = MAX | |
| $I_{CC}$ | Power Supply Current | | | | 10 | mA | $V_{CC}$ = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ($T_A$ = 25°C)

| Symbol | Parameter | Levels of Delay | Limits Min | Limits Typ | Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Address to Output | 2<br>2 | | 13<br>27 | 20<br>41 | ns | $V_{CC}$ = 5.0 V<br>$C_L$ = 15 pF |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Address to Output | 3<br>3 | | 18<br>26 | 27<br>39 | ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay $\overline{E_1}$ or $\overline{E_2}$<br>Enable to Output | 2<br>2 | | 12<br>21 | 18<br>32 | ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay $E_3$<br>Enable to Output | 3<br>3 | | 17<br>25 | 26<br>38 | ns | |

### AC WAVEFORMS

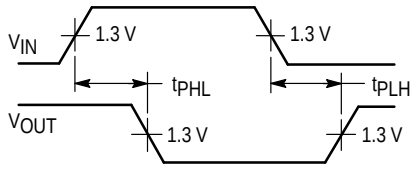



**Figure 1**

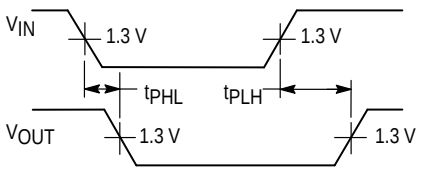



**Figure 2**